Vol. 58 • No. 2

February 2015

Microwave Journal .com

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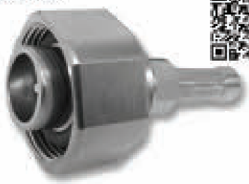
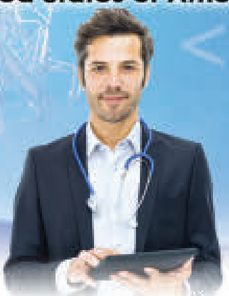
ANSYS
Electronics
Desktop



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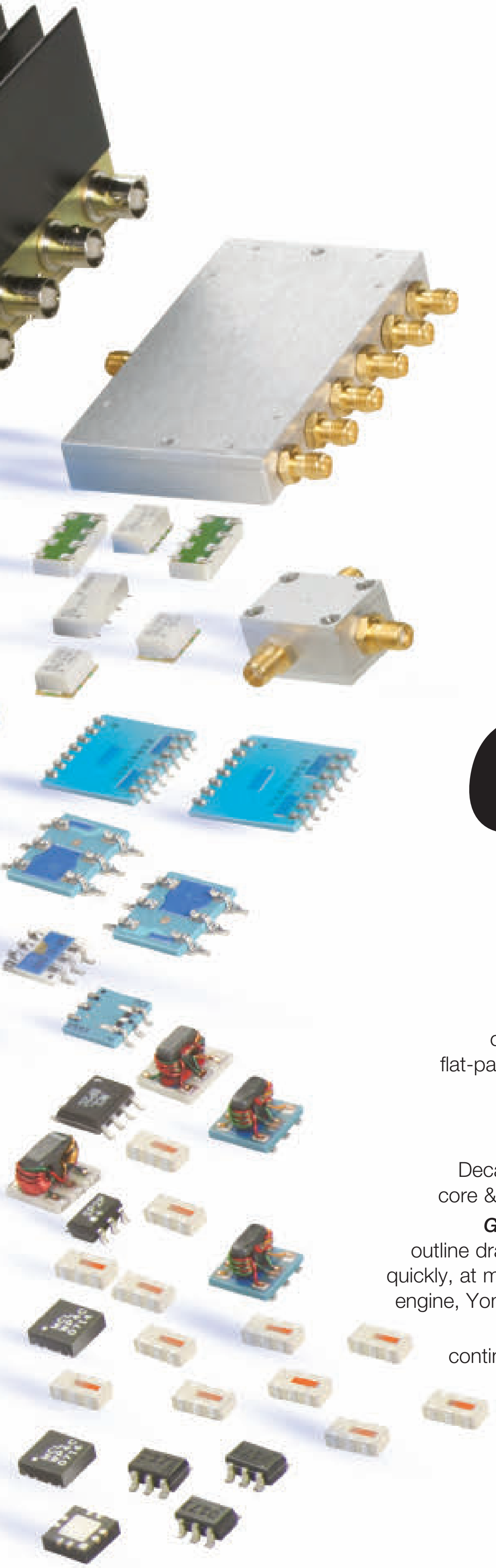
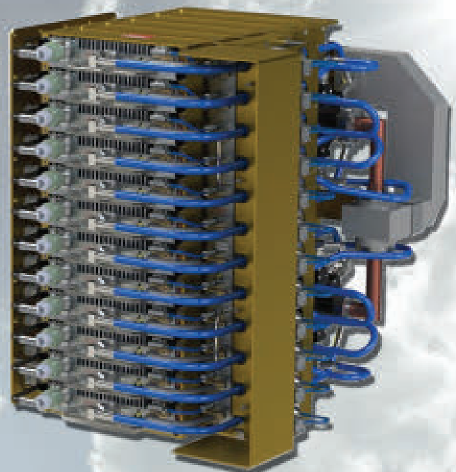
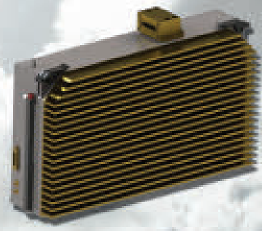
MCL
GBA-12



Solid State Power Amplifiers

S-Band



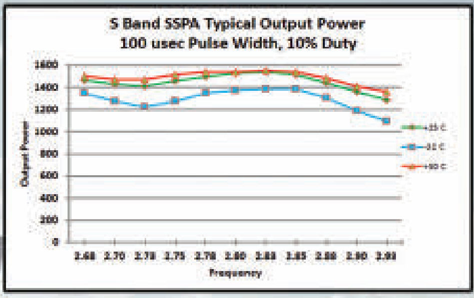


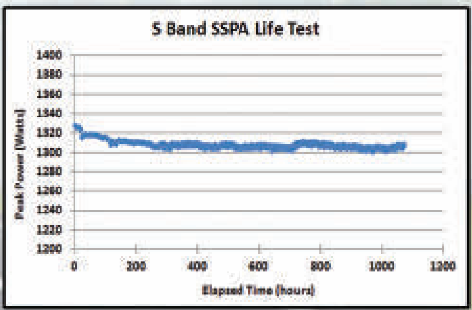
X-Band

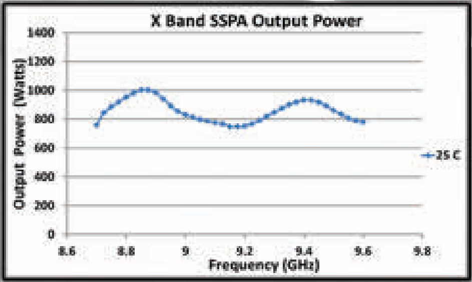
GaN Solid State Amplifiers

FEATURES

- High Efficiency Pulsed Modules (10% duty)
- BIT & Controls via - EIA 422
- Compact Light Weight
- High Reliability
- Field Replaceable Modules
- 9.0 - 9.2 GHz X-Band: 1 kW Modules
- 2.7 - 2.9 GHz S-Band: 1.3 kW Modules
- 1.2 - 1.4 GHz L-Band: 700 W Modules
- Power Combine Modules up to 25KW







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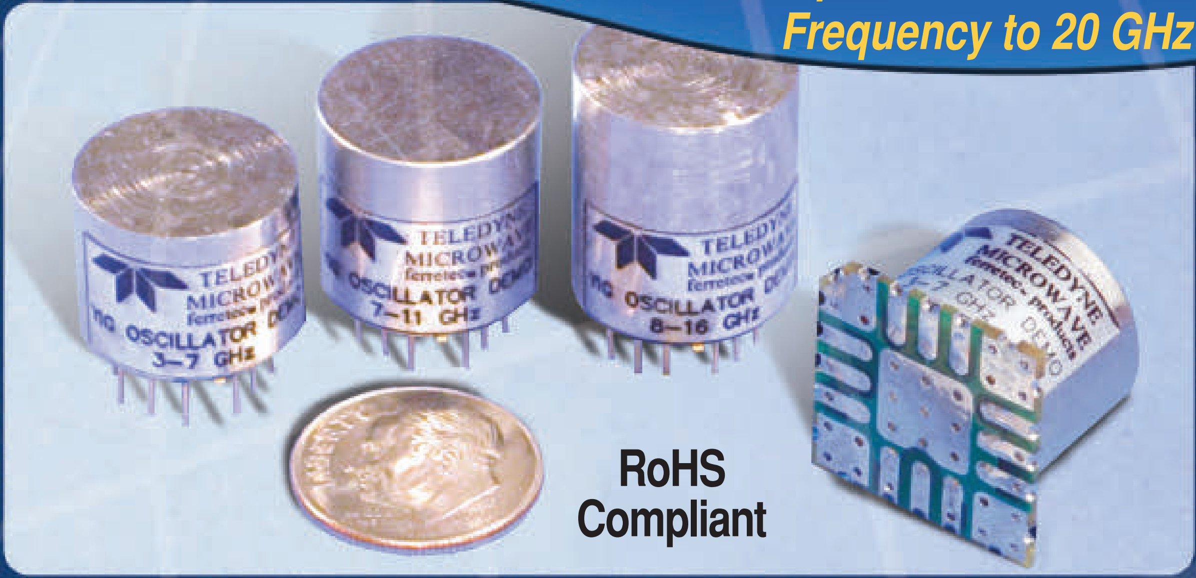
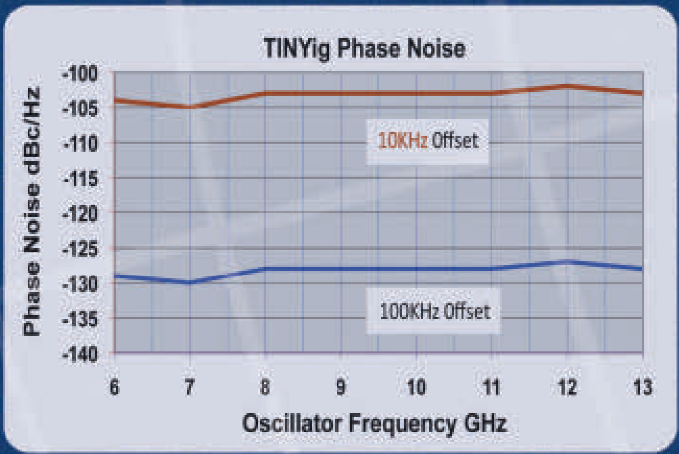
Frequency to 20 GHz





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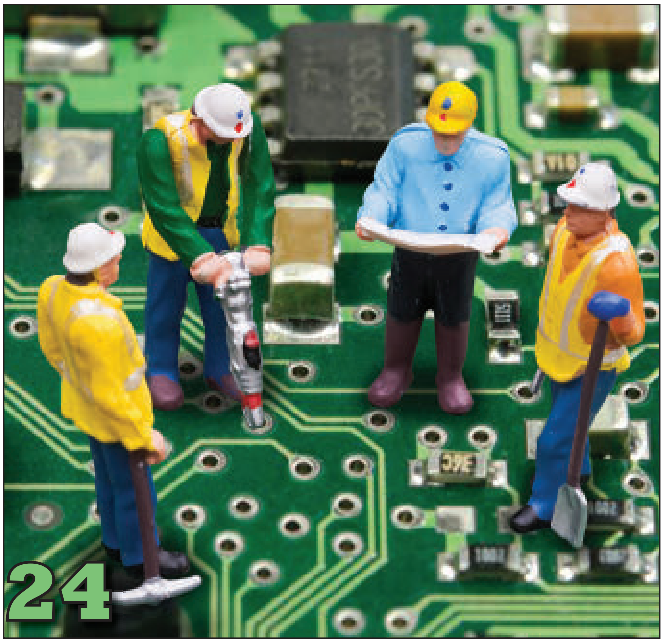

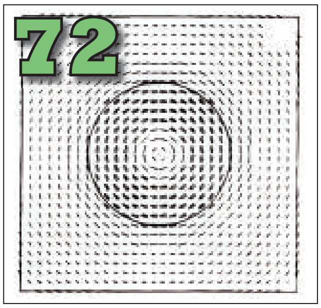

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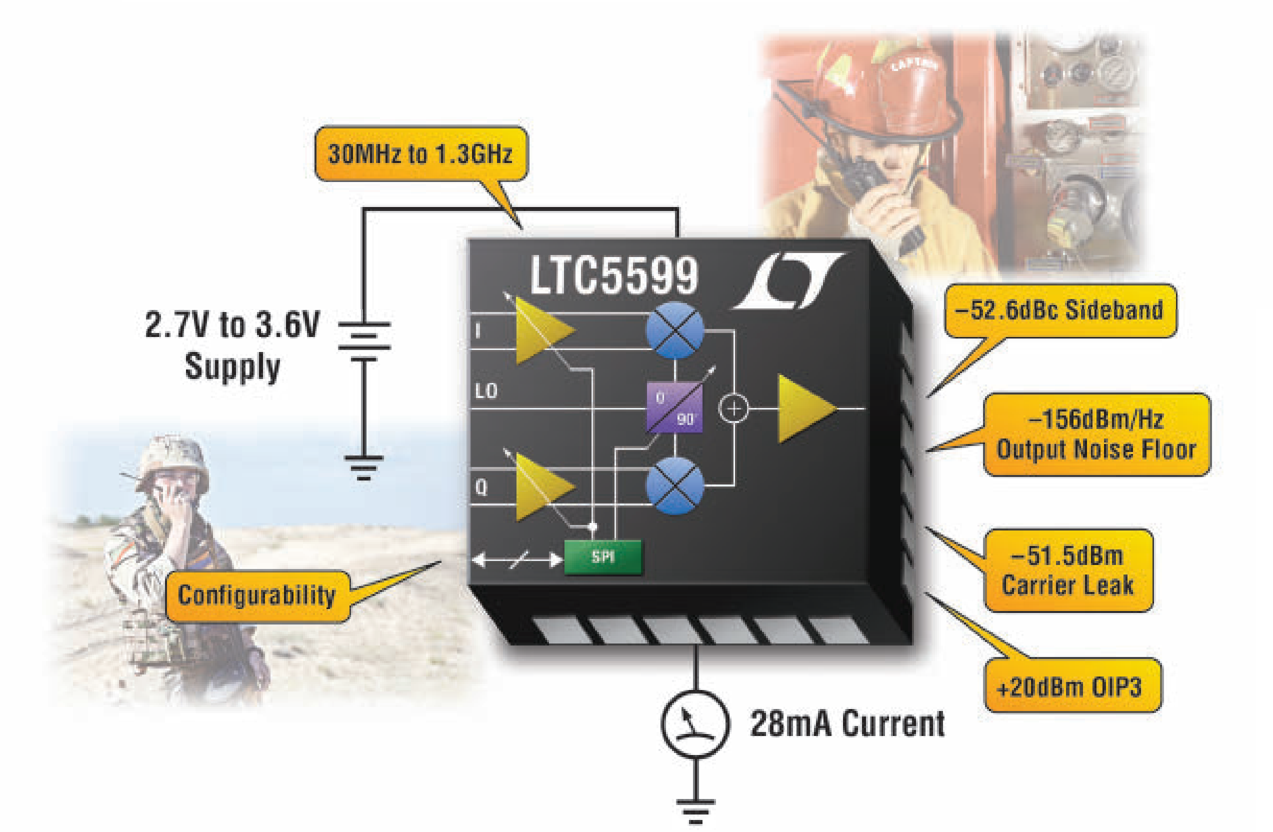
Frame the entire page in the screen and tap to experience enhancements (tap screen again for full screen view).

Refer to page 152 for this month's participants

AR pages may expire after 60 days.

58 YEARS OF PUBLISHING EXCELLENCE

90mW I/Q Modulator



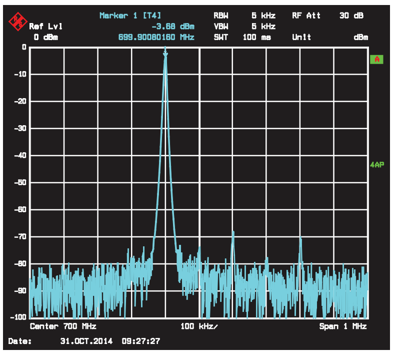
Powered from a single supply from 2.7V to 3.6V, the LTC®5599's 28mA supply current extends battery run time. The modulator offers superb –52.6dBc sideband and –51.5dBm carrier suppression—without the need of calibration. Its low noise floor of –156dBm/Hz and 20dBm OIP3 capability ensure outstanding transmitter performance. The LTC5599's built-in configurability allows users to optimize performance from 30MHz to 1.3GHz, minimizing external components and saving costs.

Features

Built-in Configurability Features:

- Gain Adjustable from 0dB to –19dB, with Supply Current Change from 35mA to 8mA
- Improves Sideband Suppression from –52.6dBc to –60dBc
- Reduces Carrier Leakage from –51.5dBm to –60dBm

Output Spectra (Optimized)



Info & Free Samples

www.linear.com/product/LTC5599

1-800-4-LINEAR

www.linear.com/solutions/5429

LINEAR TECHNOLOGY

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Transmission Line Theory and Advanced Measurements in the Field
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Tips and Techniques for Making Microwave Vector Network Analysis Measurements in the Field
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Presented by: COMSOL 2/19

Understanding Available Measurement Techniques or Unknown Signals
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Web Survey

What is your biggest PCB design challenge?

Look for our multiple choice survey online at mwjournal.com

December Survey

Where will the Internet of Things (IoT) see the most adoption over the next few years?

Environmental: monitoring air and water quality and weather conditions. [2 votes] (6%)

Infrastructure: monitoring the performance of bridges, train tracks and aircraft. [3 votes] (8%)

Energy: measuring and controlling energy use in industrial, public and residential buildings. [7 votes] (19%)

Healthcare: measuring "vital signs" and other health indicators, both in a hospital and at home. [7 votes] (19%)

Home: ensuring security and controlling lighting, heating and air conditioning. [8 votes] (22%)

Automotive: monitoring vehicle and driver performance for maintenance, safety and insurance. [9 votes] (25%)

Executive Interview

Marc A. Maury, chairman of the board of **Maury Microwave Corp.**, discusses the company's history, measurement equipment trends and product strategy for supplying everything an engineer needs in their test lab.

WHITE PAPERS

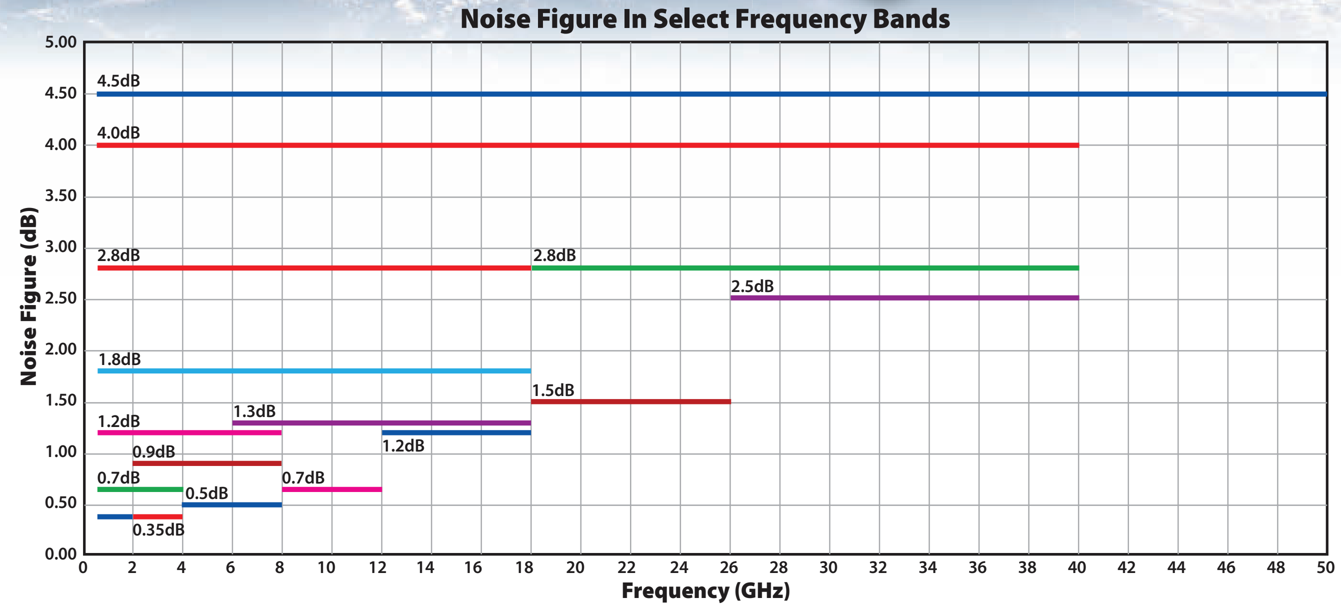
Keysight Technologies — Addressing Test Challenges for New LTE-Advanced Standard

RichardsonRFPD, An Arrow Company — Freescale's Simple Method of Changing the Frequency Range of a Power Amplifier Circuit

Catch *Frequency Matters*, the industry update from *Microwave Journal*, www.microwavejournal.com/FrequencyMatters

COM


Has Amplifier Performance or Delivery Stalled Your Program?


Noise Figure In Select Frequency Bands
Noise Figure (dB)
Frequency (GHz)
4.5dB
4.0dB
2.8dB
2.8dB
2.5dB
1.8dB
1.5dB
1.3dB
1.2dB
1.2dB
0.9dB
0.7dB
0.7dB
0.5dB
0.35dB

MARCH

MARK YOUR CALENDAR

2-5

MOBILE WORLD CONGRESS

Barcelona, Spain

This event hosts a world-class conference featuring visionary keynotes; a product and technology exhibition showcasing 1,900 companies; App Planet, the Centre of the Mobile Apps Universe; and the annual Global Mobile Awards ceremony, which recognizes mobile solutions and initiatives from around the world.

mobileworldcongress.com

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WEBINAR

ANSYS – An Insider's View of the SMAP Instrument Antenna: Major Performance and Design Details

featuring: Paola Focardi, JPL

Coming in April

EDI CON 2015

April 14-16, 2015

China National Convention Center
Beijing, China

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15-21

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Santa Clara, Calif.

EMCSI 2015 Symposium will be striving to "Keep Interference at Bay" by providing the most current information, tools and techniques on EMC testing and signal and power integrity. Join your colleagues, experts and innovators in Santa Clara, Calif. for a full week of learning, collaboration and networking.

emc2015usa.emcss.org

16-19

SATELLITE 2015

Washington, D.C.

Join more than 12,000 communications professionals in the satellite community representing 91 countries to explore next generation products and technology from more than 350 exhibiting companies.

satshow.com

16-20

IWCE 2015

IWCE INTERNATIONAL WIRELESS COMMUNICATIONS EXPO

Las Vegas, Nev.

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WEBINAR

Besser – RF and Microwave Filters

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Mini-Circuits
ISO 9001 ISO 14001 AS 9100

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WEBINAR

MicroLab – A Compact Integrated Test Facility for mm-Wave Antenna Testing

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KEYSIGHT TECHNOLOGIES

23-26

GOMACTech 2015

St. Louis, Mo.

GOMACTech is the premier forum for reporting on government funded micro and nano-electronic research and complementary efforts that focus on the technology needs of government systems.

gomactech.net

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WEBINAR

CST STUDIO SUITE 2015 Update: EDA/EMC Analysis

25

WEBINAR

CST STUDIO SUITE 2015 Update: MW&RF Simulation

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26

WEBINAR

Effect of Laminate Properties on PIM Distortion in Microstrip Transmission Lines

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Coming**Events**

CALL FOR PAPERS

NEMO 2015
February 16, 2015

ISPSD 2015
March 9, 2015

IEEE COMCAS
May 30, 2015

mwjournal.com

FEBRUARY

IDGA 2015
Military Radar Summit
February 23–25, 2015 • Washington, DC
www.militaryradarsummit.com

Scalable Active Sensor Architectures
February 24–26, 2015 • Ulm, Germany
www.iwpc.org

MARCH

GSMA Mobile World Congress
March 2–5, 2015 • Barcelona, Spain
www.mobileworldcongress.com

IEEE EMC & SI 2015
March 15–21, 2015 • Santa Clara, Calif.
www.emc2015usa.emcss.org

Satellite 2015
March 16–19, 2015 • Washington, DC
www.satshow.com

IWCE 2015
International Wireless Communications Expo
March 16–20, 2015 • Las Vegas, Nev.
www.iwceexpo.com

GOMACTech 2015
March 23–26, 2015 • St. Louis, Mo.
www.gomactech.net

APRIL

Microwave & RF 2015
April 1–2, 2015 • Paris, France
www.microwave-rf.com

WAMICON 2015
IEEE Wireless and Microwave Technology Conference
April 13–15, 2015 • Cocoa Beach, Fla.
www.wamicon.org

EDI CON 2015
Electronic Design Innovation Conference
April 14–16, 2015 • Beijing, China
www.ediconchina.com

SPACOMM 2015
7th International Conference on Advances in Satellite and Space Communications
April 19–24, 2015 • Barcelona, Spain
www.iaria.org

MAY

AUVSI's Unmanned Systems 2015
May 4–7, 2015 • Atlanta, Ga.
www.auvsi.org

ISPSD 2015
International Symposium on Power Semiconductor Devices and ICs
May 10–14, 2015 • Hong Kong, China
www.ispsd2015.com

RFIC 2015
IEEE Radio Frequency Circuits Symposium
May 17–19, 2015 • Phoenix, Ariz.
www.rfic-ieee.org

IMS 2015
IEEE MTT-S International Microwave Symposium
May 17–22, 2015 • Phoenix, Ariz.
www.ims2015.org

CS Mantech 2015
May 18–21, 2015 • Scottsdale, Ariz.
www.csmantech.org

Space Tech Expo 2015
May 19–21, 2015 • Long Beach, Calif.
www.spacetechexpo.com

Aerospace Electrical Systems Expo 2015
May 19–21, 2015 • Long Beach, Calif.
www.aesexpo.com

85th ARFTG Microwave Measurement Symposium
May 22, 2015 • Phoenix, Ariz.
www.arftg.org

EW Europe 2015
May 26–28, 2015 • Stockholm, Sweden
www.eweurope.com

JUNE

Sensors Expo & Conference 2015
June 9–11, 2015 • Long Beach, Calif.
www.sensorsexpo.com

AUGUST

EMC 2015
International Symposium on Electromagnetic Capability
August 16–22, 2015 • Dresden, Germany
www.emc2015.org

EDI CON Seeing Double

Pat Hindle
Microwave Journal *Editor*

In its third year, EDI CON China has the most exciting conference schedule ever. Taking place April 14-16 at the China National Convention Center (CNCC) in Beijing, the conference and exhibition will feature the latest practical sessions and workshops on popular topics such as IoT device design/characterization, GaN amplifier design, envelope tracking & DPD modeling/design, radar design/analysis, PCB design/characterization, WLAN design/measurement, MIMO design/testing, EMI modeling/testing and high speed design.

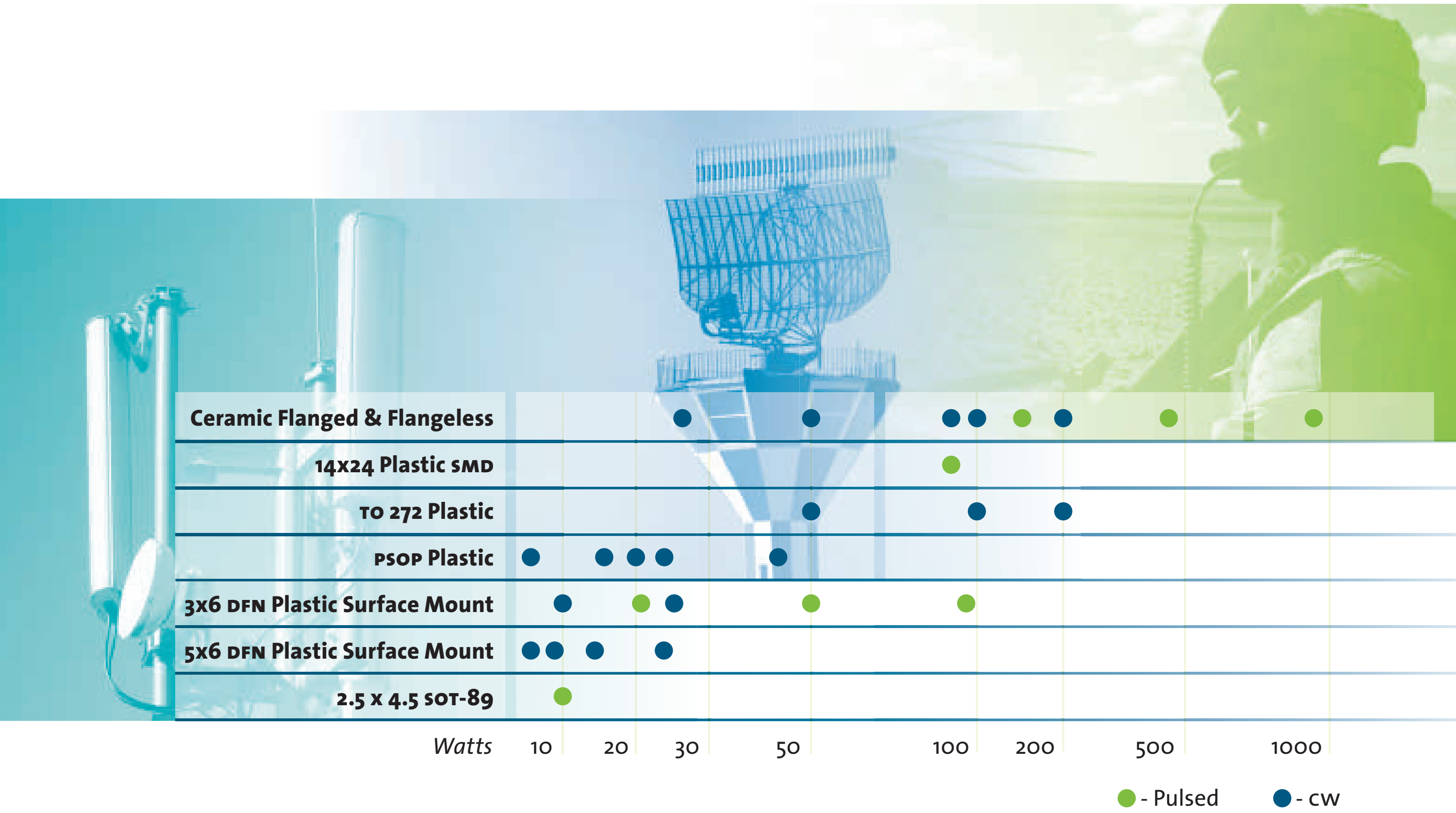
New this year is a full day 5G Forum that will include a plenary session from China Mobile about their outlook on 5G advanced communications technologies, followed by a panel session with experts from China Mobile, Shanghai Tech, Keysight Technologies, Rohde & Schwarz, National Instruments and MACOM. A series of eight sessions and two workshops will cover topics such as massive MIMO, HetNets, phased array transceivers, timing and synchronization, testing challenges, new modulation schemes and mmWave technologies.

Following the morning paper sessions on the first day will be a set of workshops before the afternoon plenary talks and VIP reception dinner. A couple of noteworthy tracks include amplifier design techniques with several talks on envelope tracking and another track on high frequency PCB design. The plenary talks will kick off with honorary Chairman, Professor Junde Song from Beijing University of Posts and Telecoms, discussing "Smart Cities and Communities." Other scheduled speakers include Hongbing Ma from China Unicom discussing 5G future communications technologies and Wei Chen from China Mobile discussing IoT. The three major EDI CON sponsors will also speak with representatives from Keysight Technologies, Rohde & Schwarz and National Instruments covering their latest technologies and innovations. The Keysight sponsored VIP reception dinner will take place on-site shortly after the plenary talks. The second day has full day tracks focused on radar, IoT, systems design and high speed/EMI measurement and modeling. The third day will have a full morning of sessions with one set of workshops in the afternoon prior to the awards ceremony for best posters and papers.

The exhibition is bigger than ever with more than 100 companies participating. In addition to the three major sponsors, gold level sponsors include Mini-Circuits, Anritsu, Richardson RFPD/Arrow, CST, RFHIC and CETC41. These companies will be giving workshops on various topics along with ANSYS, MACOM, Peregrine, Gore, Rogers, Freescale, Arlon, H+S, Radiall, Win, Qorvo, Focus, Farran, Tektronix and Transemic. Workshops will cover various test & measurement and modeling solutions to today's engineering challenges in amplifier design, envelope tracking and DPD, radar, EMI/EMC, LTE, 5G, MIMO/massive MIMO and IoT. Materials companies such as Rogers and Arlon will be discussing PCB design and cable/connectors companies such as H+S, Radiall and Gore will be covering connector design and cable solutions for testing and other high performance applications. Semiconductor solutions companies such as Richardson RFPD/Arrow, RFHIC, Freescale, MACOM, Peregrine, Transemic, NXP, WIN and Qorvo will be doing workshops on switching, filtering and amplifier solutions.

The EDI CON model with its practical, industry driven sessions and workshops has proven so successful that *Microwave Journal* and Horizon House are launching EDI CON USA in 2016, taking place September 20-22 in Boston, Mass. at the Hynes Convention Center. With all of its rich electronic design activity and history, the New England area is the perfect place to hold the first EDI CON USA event. EDI CON USA will partner with Keysight Technologies, as they do with EDI CON China, as their host sponsor and will offer key sponsorships to its other EDI CON China partners such as Rohde & Schwarz, National Instruments, Mini-Circuits, Anritsu, Richardson RFPD, CST, ANSYS and RFHIC. The first EDI CON USA event hopes to draw thousands of engineers from its sponsors, international electronic design companies and local New England companies such as Raytheon, BAE Systems, Mercury Systems, Cobham, Skyworks, MACOM, Qorvo, ADI/Hittite and Rogers Corp. Other future locations with large, high frequency design communities will be considered for future EDI CON USA events.

It is going to be an exciting year with hot beds of activity already taking place in areas such as IoT, 5G, radar and UAVs. *Microwave Journal* will strive to bring you the best articles, webinars and conferences to keep you informed about the latest technologies and techniques being developed throughout the industry. ■



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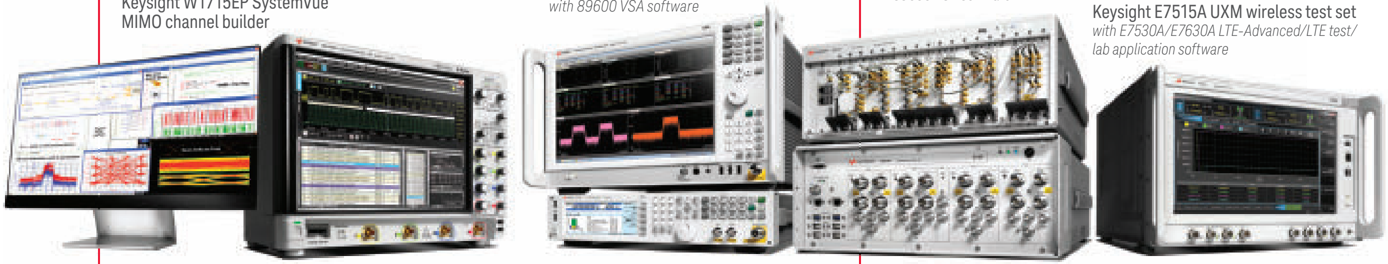
Keysight W1715EP SystemVue
MIMO channel builder

Keysight N9040B UXA signal analyzer
with 89600 VSA software

Keysight MIMO PXI test solution
with N7624/25B Signal Studio software for LTE-Advanced/LTE FDD/TDD and 89600 VSA software

Keysight E7515A UXM wireless test set
with E7530A/E7630A LTE-Advanced/LTE test/lab application software



Keysight Infiniium S-Series high-definition oscilloscope
with N8807A MIPI DigRF v4 (M-PHY) protocol decode software

Keysight N5182B MXG X-Series RF vector signal generator
with N7624/25B Signal Studio software for LTE-Advanced/LTE FDD/TDD

Keysight E6640B EXM wireless test set
with V9080/82B LTE FDD/TDD measurement applications and N7624/25B Signal Studio software for LTE-Advanced/LTE FDD/TDD

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KEYSIGHT TECHNOLOGIES

Unlocking Measurement Insights

Cover Feature
Invited Paper

New Thermoset PCB Material Emerging for mmWave Applications

Tarun Amla
Isola Group, Chandler, Ariz.

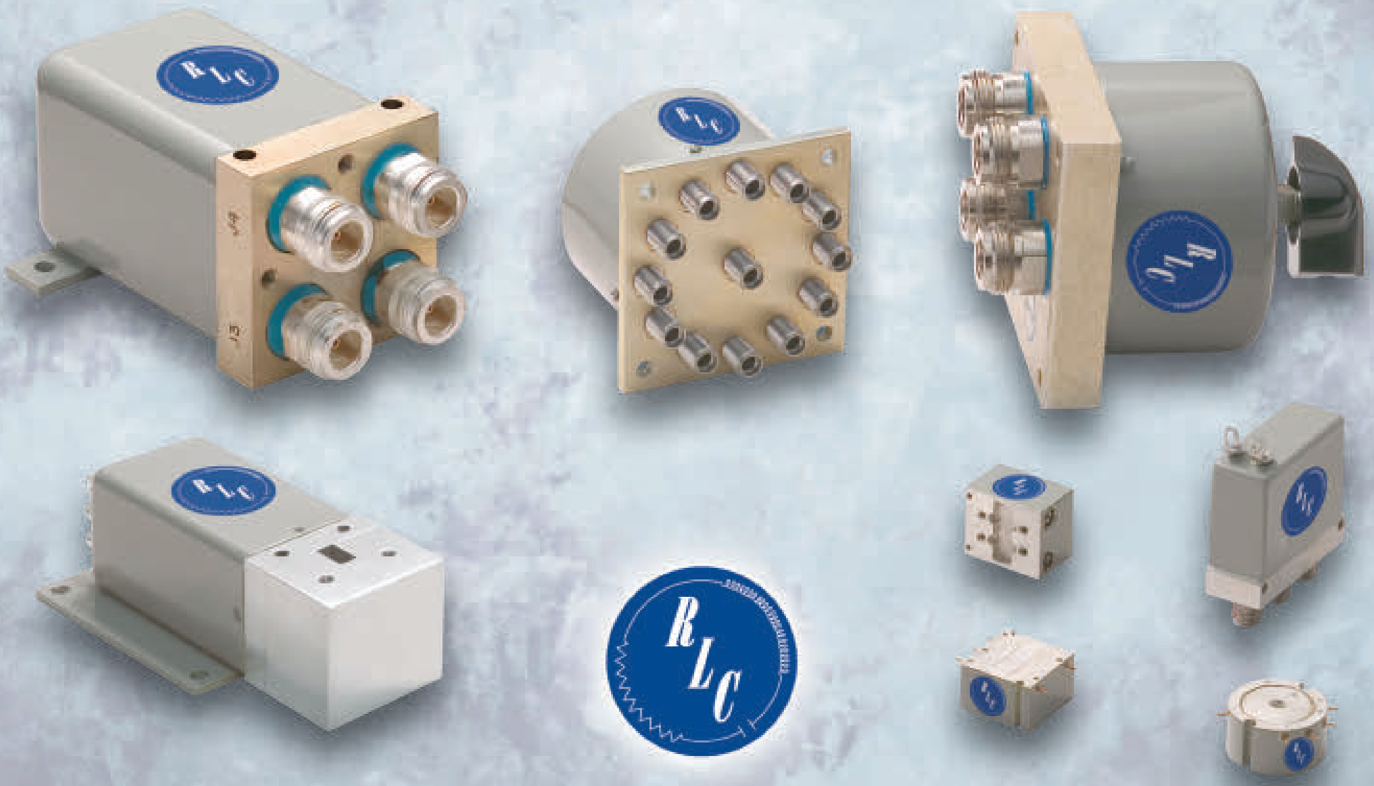
Requirements for stability of dielectric properties, manufacturability and suitability for use in hybrid technologies highlight deficiencies in current material solutions. The industry must break from its dependence on the polytetraflouroethylene (PTFE) and highly filled hydrocarbon based material solutions towards a newer set of high glass transition temperature (T_g) thermoset materials introduced to address current and future material needs.

Radio frequency printed circuit boards are typically manufactured using thermoplastic substrates such as PTFE or filled hydrocarbon based resins. These resins have excellent electrical properties but poor mechanical and thermo mechanical qualities. With the advent of new material technologies, there is a growing emphasis on the mechanical and thermal characteristics of the dielectrics as well as their electrical properties. Emerging product technologies require multilayer circuitry, hybrid RF/digital technology and increased power handling capability to be engineered into substrates.

EMERGING APPLICATIONS

Aerospace and defense applications have historically been the foundation for development of RF and millimeter wave technologies. In recent years, however, there has been a massive increase in commercial RF applications. With the widespread proliferation of wireless communications, commercial RF applications have grown exponentially and are moving higher in frequency. Automotive radar for example, is increasing in frequency of operation from K-Band to W-Band. V-Band ultra-broadband wireless indoor communications, microwave imaging at 94 GHz and applications at other millimeter wave frequencies are being developed as well.[1] Multiple functions are integrated on single chips facilitating board integration, while exacerbating thermal management issues.

V-Band point-to-point microwave links are emerging as environmentally friendly alternatives to fiber-to-home technologies. In the U.S., U.K. and some Asian countries, the frequency band from 56 to 64 GHz is not regulated, providing opportunities for deployment of point-to-point, line of sight links with very high bandwidth and frequency reuse capability. This frequency band is known for high attenuation caused by oxygen in the atmosphere and does not allow the signal to propagate beyond a certain distance, making the communication more secure. The use of turbo coding and signal processing techniques such as the Viterbi algorithms has caused the communication bandwidths to approach the theoretical Shannon limit and the focus is now on increasing the bandwidth through smaller cells.[2] These networks comprised of macro base stations coupled with micro, femto and picocells form heterogeneous networks, or HetNets. HetNets rely on very small cells which can cater to a group, office, building or a set of buildings. The communication is mainly digital and could



be fed through point-to-point links or wireless links.[2] The circuitry required is hybrid to a certain extent with RF or digital on the receiving or transmitting end. These heterogeneous networks are being looked at as a solution to increasing capacity and improving network coverage.

Millimeter wave frequencies present unique challenges for PCB materials. Methods and techniques are not established or standardized for measuring the dielectric properties in millimeter wave region. RF/microwave integration into ICs also affects how these materials are used.

PCB REQUIREMENTS

Dielectric material properties are driven by system requirements such as frequency of operation, power handling, noise, size, types of components and features. Dielectric loss, thermal stability and thermal management requirements, layer count, modulus, warp and twist requirements, and other factors go into the selection of the appropriate PCB material. Stability with humidity and temperature, power handling capability and passive intermodulation (PIM) have a bearing on material selection as well.

In addition to dielectric losses, conductor losses are becoming increasingly important. The surface roughness of copper plays a major role in increased attenuation at higher frequencies and especially in the millimeter wave region where conductor losses can dwarf dielectric losses. The skin depth at frequencies around 77 GHz is extremely small so most of the current must flow through the surface where it is strongly influenced by roughness. ***Figure 1*** shows the surface roughness of the different types of copper used. Skin depth as a function of frequency and the effect of copper surface roughness on relative attenuation are shown in ***Figures 2*** and ***3***, respectively. Figure 3 was developed using the Hammerstad and Bekkadal equation.[3]

$$\alpha_c' = \alpha_c \left\{1+\frac{2}{\pi}\tan^{-1}\left[1.4\left(\frac{\Delta}{\delta_s}\right)^2\right]\right\} \quad (1)$$

where Δ = root mean square surface height, δ_s = skin depth and α_c = conductor loss.

PIM occurs in passive devices whenever RF signals at two or more frequencies are present on a conductor. PIM is created by superimposing sine waves, creating harmonics that can add, subtract, or even cancel the desired signal. PIM causes unwanted noise, increasing the signal to noise ratio. Odd harmonics can generate spurious signals that can lead to communications interference and disruption. The use of appropriate copper with very low impurities and low roughness helps alleviate PIM.

PCBs for RF applications are typically double sided or of hybrid (multilayer/dissimilar dielectric) construction. Hybrid PCBs, consisting of FR-4 and RF optimized substrates reduce the overall cost of materials. They are typically used for power amplifiers in

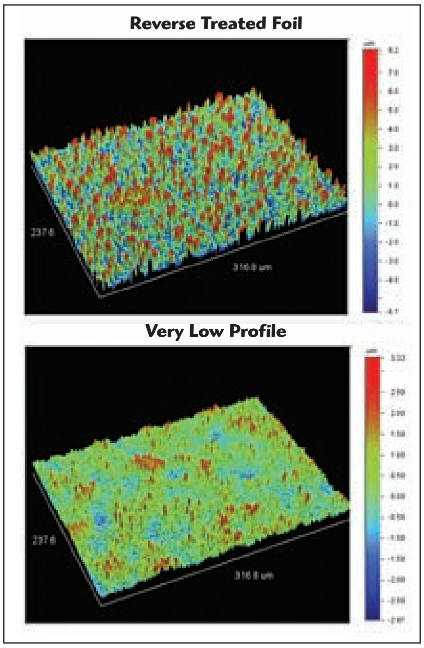


Fig. 1 Comparison of the roughness of reverse treated foil (RTF) and very low profile (VLP) copper. The RTF has a root-mean-square roughness (Rrms) of 0.59 µm, with maximum height (Rz) of 3.93 µm. The VLP is better, with Rrms = 0.36 µm and Rz = 2.06 µm.

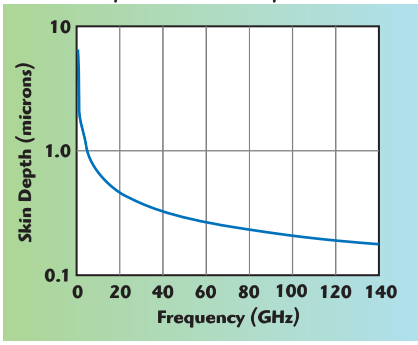


Fig. 2 Skin depth as a function of frequency.

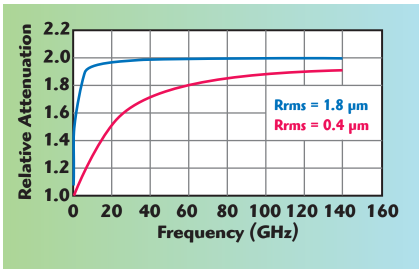


Fig. 3 Relative attenuation as a function of copper surface roughness.

cellular base stations, low noise block down converters and advanced automotive safety systems.

Chip manufacturers are packing more functionality into ICs, driving the need for PCB materials that meet both high speed digital and RF requirements. This includes predictable dimensional stability, low loss, controlled dielectric constant, lead-free construction with very tight pitches and electrochemical migration (or conductive anodic filamentation) resistance. CAF poses a major reliability risk by creating a conductive path between holes, or holes and planes.

There is an emerging need for isotropic RF substrates with higher thermal conductivity. RF boards will also see new requirements for CAF and thermal cycling reliability. PCB processes such as drilling and plating are coming under increased scrutiny to ensure reliable performance. These new requirements, coupled with the existing material challenges make RF board manufacturing increasingly more complex.

TABLE 1

PROPERTIES OF PTFE

Property	Value	Units
Density	2100 to 2300	kg/m^3
Melting Point	327	°C
CTE	135	$\times 10^{-6}$m/m/°C
Young's Modulus	0.5	GPa
Yield Strength	23	MPa
Thermal Conductivity	0.25	W/m-°K
Poisson Ratio	0.46	
ε_r	2.1 to 2.3	
Tan δ	< 0.001	
γ-transition	-100	°C
β-transition	20	°C
α-transition	127	°C

CURRENT PCB MATERIALS

Most dielectrics in use today are based on PTFE or highly filled hydrocarbon based resins. Another new class of products employs conventional thermoset technology to produce high glass transition polymer composites for use in these emerging applications.

PTFE/PTFE with Woven Fabrics/ Filled PTFE Based Dielectrics

PTFE is a long chain polymer of high molecular weight. It is primarily crystalline in nature.[4] It is in wide use for RF applications because of its superior electrical properties, having a low dielectric constant between 2.1 and 2.3 and a loss tangent below 0.001. These properties are stable up to millimeter wave frequencies. PTFE is traditionally used as a substrate for RF applications, including applications in space. ***Table 1*** summarizes its properties.

Dielectric Properties: It is commonly believed that the dielectric properties of PTFE are very stable with temperature; however, there is variation. To understand this, one must look at its structure. PTFE after polymerization is almost 90 to 95 percent crystalline. Cooling down and further processing determines the degree of crystallinity at room temperature. Processing steps, such as sintering above its melting point, lead to changes in crystallinity. PTFE has a crystalline melting point at an atmospheric pressure of about 332° to 346°C for unsintered material and about 327°C for sintered material. For 100 percent crystalline PTFE, relative densities of 2.347 at 0° and 2.302 at 25°C have been calculated from the x-ray crystallographic data. The relative density of amorphous PTFE is 2.00, as obtained by density measurements at room temperature.[4] Almost all fabricated PTFE displays crystallinity within the range of 50 to 75 percent depending on the rate of cooling. The relative density of 100 percent crystalline PTFE at 23°C is 2.3 while that of 0 percent crystalline (100 percent amorphous) PTFE under the same conditions is 2.0. Therefore, the relative density of PTFE can be used to provide a simple index of crystallinity. The dielectric loss of PTFE is sufficiently low to allow the permittivity to be calculated with a high degree of accuracy using the Clausius-Mossotti formula.[4,5]

$$\frac{\varepsilon-1}{\varepsilon+2}=\frac{\rho N_A\alpha}{M_W 3\varepsilon_0} \quad (2)$$

where NA is Avogadro's number and the quantity $\frac{N_A\alpha}{3\varepsilon_0}$ is called the molar polarization (P_M) and has dimensions of volume. The values for bond polarizabilities can be looked up or added up using group contributions methods.

$$\frac{\varepsilon-1}{\varepsilon+2}=k\rho \quad (3)$$

Using this expression with a k value of 0.125,[5-7] is valid only for non-polar molecules. ***Figure 4*** shows the relationship between the density of PTFE and ε_r. Stability of the dielectric constant depends on the density of PTFE which changes with temperature, so the properties of PTFE are not as stable as often portrayed. The sintering process required for building the circuit boards will change the density.

Mechanical Properties and Creep: PTFE has a low elastic modulus of about 0.5 GPa. The coefficient of thermal expansion (CTE) is also highly variable and shows very high expansion. Until now PTFE has been the material of choice for use at millimeter wave frequencies. While PTFE may be today's workhorse, it may not be the best choice for future applications due to issues with its mechanical and physical properties. At high temperatures, permanent deformation can occur over time at a stress level well below its yield strength. This time-dependent permanent deformation is called creep. It occurs at low stress levels and a temperature above $0.5T_m$, where T_m is the absolute melting point. A polymer such as PTFE, which has a 600°K melting point, would experience creep at over 300°K or 27°C (close to room temperature). Creep is measured by loading at a constant stress level and measuring the deformation over time. Initial elastic and primary creep occur very quickly and then the creep develops at a steady state rate followed by a very steep rise leading to fracture.[8] PTFE is highly prone to creep, which raises doubt concerning its suitability for demanding environments such as automotive applications that require operation in temperatures from subzero to close to 85°C. Steady state creep strain can be expressed as

$$\dot{\varepsilon}_{ss}=B\sigma^n \quad (4)$$

$$\dot{\varepsilon}_{ss}=\varepsilon_0\left(\frac{\sigma^n}{\sigma_0^n}\right)e^{-\left(\frac{Q_c}{RT}\right)} \quad (5)$$

where B is a constant, n is a value between 3 and 8, Q_c is the activation energy in J/mol and R is the universal gas constant in J/mol/k. This equation with an exponent, n, of around 5 indicates that the creep rate can double with a modest increase of 20°C.[9] The creep rate of PTFE materials makes them unsuitable for applications requiring higher temperatures as it would cause a shift in the dielectric properties.

Processing Challenges: PTFE based materials are regarded as less desirable for multilayer PCBs due to

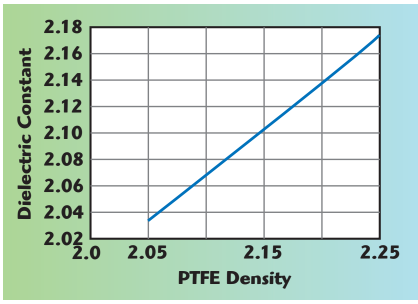


Fig. 4 PTFE dielectric constant versus density.

their high cost, high CTE and processing difficulties. Therefore, the use of PTFE based laminates has been relegated to lower layer count boards. PTFE requires very high processing temperatures over 330°C and high pressure. The bonding sheets are not available and there is no flow or fill to encapsulate the traces and the circuitry. Most PTFE based laminates are available as microfiber filled sheets and therefore possess very low elastic moduli. Some laminates with dielectric constants above 3.2 use woven glass reinforcement, but this increases the dissipation factor due to the use of glass. Non-reinforced PTFE has a lower dielectric constant and dissipation factor, but due to its low modulus and very high CTE, it must be filled with ceramic fillers. Because the PTFE materials do not really bond to the filler particles and simply encapsulate them, the net effect is a reduction in PTFE polymer volume, while the overall CTE is not significantly lowered. High CTE can lead to issues

such as dimensional deformation, inter-laminar shear stress when building hybrids and/or residual stresses in the board. As creep manifests itself over a longer period of time, the stress continues to relax at room temperature. This can lead to the product not performing at the optimum level over time due to creep-induced deformation. High CTE in the Z axis affects plated-through-hole reliability. Copper has a low coefficient of expansion and the mismatch leads to stresses causing fatigue failure as copper experiences high plastic strains.

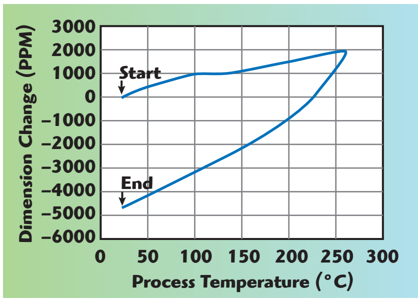
Technology is shifting towards higher layer counts and sequential laminations for mixed RF/digital boards. The technology shift creates constraints on expansion; this means CTE is of special importance for these multilayer designs. Registration is of high importance as well, because of smaller pitches and pad sizes that rely on plated through-holes to create connections between the different PCB layers. PTFE laminates filled with abrasive fillers lead to high drill wear and are generally more difficult to drill. The drill bit life is substantially reduced, increasing manufacturing costs.

Dimensional Stability: The main issue with PTFE substrates is poor dimensional stability. Due to its low glass transition temperature and low yield strength, it exhibits a high degree of permanent plastic deformation. ***Figures 5*** and ***6*** show deformation of a glass microfiber-filled material in the X- and Y- directions. Permanent deformation is very high, almost an order of magnitude higher than for FR-4 products. Manufacturing boards with acceptable yields is difficult and expensive. This is the single biggest challenge to using PTFE based laminates for hybrid or multilayer applications.

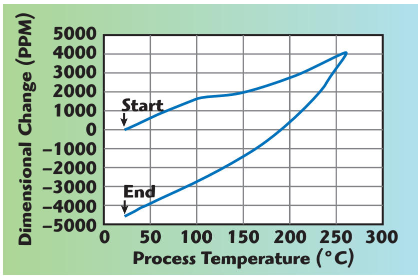
Highly Filled Hydrocarbon Based Resins

Hydrocarbon based resins are cross linked with other polymers to increase the T_g, but while they are are presented as high T_g materials, they have intrinsically very low T_gs. Typically, when measured using a dynamic mechanical analyzer (DMA), they will exhibit a glass transition of around 95° to 105°C. The numbers with differential scanning calorimetry (DSC) cannot be read as there is not a significant transition signal due to the amount of filler used. A thermo-mechanical analyzer (TMA) shows no inflection on the Z-axis expansion at higher temperatures but an inflection can be observed in the sub-ambient to 60°C range. This indicates a very high filler loading on a woven glass fabric with a rubbery low T_g matrix.

These laminates are used in applications such as base stations and LNBs. Since they do not have the low loss properties of PTFE or the adhesion required for the use of low profile copper, their use will be limited. Dielectric properties are not stable with temperature and have been known to shift due to oxidation under operation at modestly elevated temperatures. In fact, the



▲ *Fig. 5 X-direction dimensional change versus temperature of microfiber filled PTFE.*



▲ *Fig. 6 Y-direction dimensional change versus temperature of microfiber filled PTFE.*

laminates offered as oxidation resistant show severe discoloration upon exposure to elevated temperatures. The fillers are highly abrasive and lead to drilling issues. The drilling costs sometimes are higher than the cost of the material itself. Additional processing steps, such as plasma drilling for hole wall preparation, are expensive. The product offering does not include bonding sheets; limited offering is available for cores.

The other major issue is CTE mismatch in the building of hybrids. Because the resin matrix is highly filled, the CTE in the Z-direction is very low. Additionally, as there is no T_g above

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60°C, the X and Y CTEs do not show an inflection and continue expanding at the same rate. The FR-4 type laminates undergo a transition and show a sharp increase in Z expansion and a significant drop in X and Y CTEs. When bonded together, the hybrid board experiences strain, leading to high thermal stress between the FR-4 and the ceramic filled laminates. This often results in de-lamination.

The inability to make robust hybrid boards, lack of suitable bonding sheets, higher loss, inability to use extremely low profile copper, and low dielectric stability under elevated temperature, coupled with oxidation risks will render these types of products obsolete as technology shifts to higher layer counts.

A NEW CLASS OF THERMOSET POLYMERS

Over the last few years, the market has witnessed the arrival of thermoset materials that behave like standard FR-4 materials, while delivering excellent electrical and thermo-mechanical properties. The products are thermoset systems exhibiting a T_g of around 200°C. CTEs are well controlled even for higher resin constructions. A full complement of laminates and prepregs is available including an offering for the high speed digital and RF and millimeter wave space. The products are available in a full range of dielectric constants.

Stability of Dielectric Properties Over Frequency

Dielectric properties are stable from 1 to over 100 GHz. Virtually no change is detected over the entire range. This is attributed to the fact that the products are truly high T_g thermoset polymers and therefore do not exhibit inflections in crystallinity like PTFE or the artifacts of low T_g with the highly filled hydrocarbon based resin systems. ***Figure 7*** shows the data generated by IZM Fraunhofer Institute in the 102 to 103 GHz range. The properties are very stable and the dielectric constant and dissipation factors are virtually unchanged at high temperature.

One of the major concerns with the dielectrics is the ability to retain their properties after prolonged exposure to high temperature. Continuous operation at 85° to 125°C is a fairly common requirement. Even minor changes in


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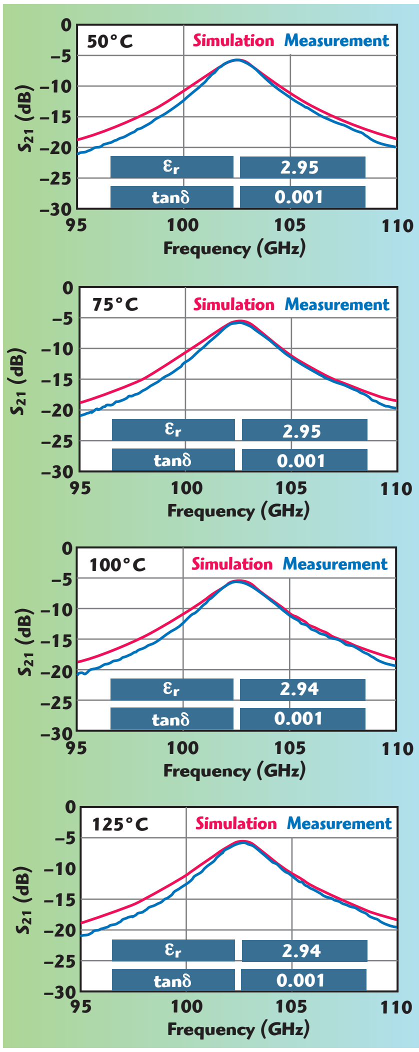
dielectric properties can lead to major performance issues. As shown in ***Figures 8*** and ***9***, the high T_g thermoset systems, even after prolonged exposure to high temperatures, show little or no oxidative or other degradation. Changes in dielectric properties are minimal in comparison to the PTFE or highly filled hydrocarbon based products.

Insertion Loss and Power Handling

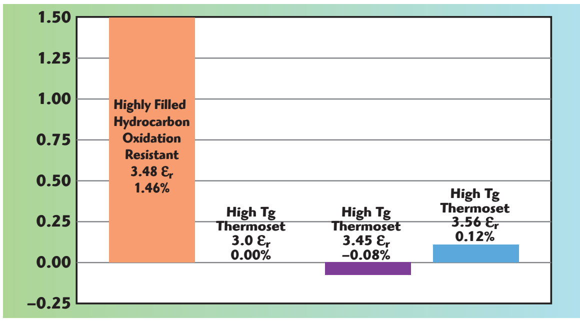
Conductor loss not only contributes to overall loss but also increases power dissipated into the board, leading to undesirable temperature increases and power handling limitations. Due to conductor surface roughness, there is also an increase in parasitic capacitance; and the phase constant (β) changes with frequency affecting phase velocity and group velocity as well.[10] The solution is to use as low a profile of copper as possible. However, this is not straightforward because the resin system must bond securely with very low profile copper, without requiring any special treatment.

The newer thermoset systems are unique in the sense that they provide high peel strengths even for the smoothest copper available. These products are more advantageous for millimeter wave applications, as extremely low profile copper with R_z values below 1.5 μ can be used. These R_z values are lower than the rolled annealed copper that was once considered the benchmark. The rolled annealed copper is only available in small formats and requires special treatment for bonding.

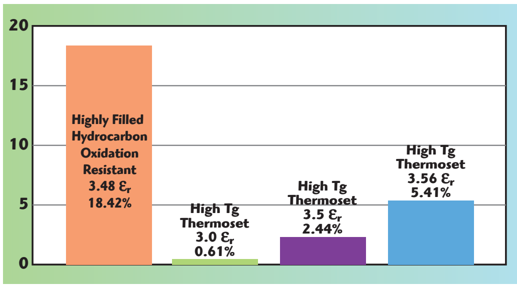
With low profile copper, insertion loss goes down substantially. Energy from conductor and dielectric loss is dissipated in the dielectric, leading to dielectric heating.[3,11,12] Reduced conductor loss, therefore, increases the



▲ *Fig. 7 Simulated and measured RF properties of new thermoset material at various temperatures. Data courtesy of IZM Fraunhofer.*



▲ *Fig. 8 Change in dielectric constant for various materials, measured at 10 GHz following 1000 hours of aging at 125°C.*



▲ *Fig. 9 Change in dielectric loss for various materials, measured at 10 GHz following 1000 hours of aging at 125°C.*

power handling capability. ***Figure 10*** compares a high T_g thermoset transmission line with one using a filled (non woven) PTFE dielectric. The power handling capability of microstrip lines can be obtained by taking Equation 11, and setting the thickness d=0.[11]

$$\Delta T = T - T_{amb} =$$

$$\frac{.2303h}{K}\left[\frac{\alpha_c}{w_e} + \frac{\alpha_d}{2w_e(f)}\right] \text{in} \frac{^\circ C}{w} \qquad (6)$$

where K is the dielectric thermal conductivity W/m-°K, α_c , α_d are the conductor and dielectric losses, w_e is the effective width and h is the height, average power handling is given by

$$APH = \frac{T_{max} - T_{amb}}{\Delta T} W \qquad (7)$$

Figure 11 compares the power handling of a filled PTFE microstrip line with that of a high T_g thermoset low loss microstrip line. Higher power handling in the thermoset PCB is enabled by its higher thermal conductivity and use of very smooth, high peel strength copper.

Processing and Cost of Ownership

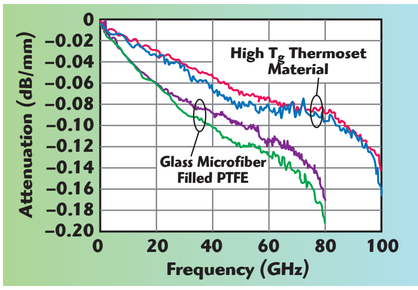
The ease of processing and availability of choices is a big factor in the fast adoption of these new products. Dimensional stability is very predictable, leading to high yields. Drilling costs are much lower due to the fact that the products have low filler loading. The melt viscosity is in the same range as FR-4 type systems with similar flow and fill behavior. Processing does not require the use of plasma; the standard desmear process is suitable.

Because CTEs are in the same range as standard FR-4 materials, with similar thermo-mechanical properties, the ability to make reliable hybrid boards is straightforward. Creep does not manifest itself as the T_g, at 200°C, is sufficiently high. A number of OEMs are adopting these products for automotive radars, phased array antennas, sensors, base station power amplifier boards and other RF applications. Customers are reporting significant cost savings.

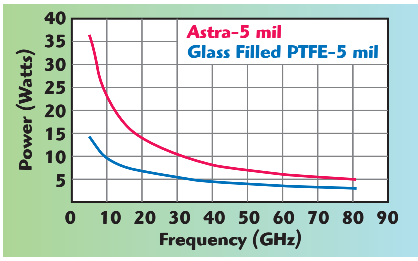
CONCLUSION

A new enabling technology employs a thermoset matrix that has very good adhesion to metals, enabling the use of copper with extremely smooth surfaces. The industry is increasingly seeing hybrid boards combining RF and digital technology. The increasing integration of functionality into single chips is making it easier to combine the digital and RF circuitry on the same board. Conventional RF substrates such as PTFE are not suitable for hybrid technology, as the layer count is high and bonding sheets are not available. Also, the manufacturing costs of boards made using PTFE or the hydrocarbon based resin alternatives are high. Yields are poor due to the dimensional stability issues, and the systems tend to be unreliable.

There is a strong need for non-PTFE and non-thermoplastic based substrates with dielectric properties similar to PTFE. Thermoset systems, which display high glass transition temperatures and high thermal reliability, while maintaining stability in dielectric properties over a higher range of temperatures and frequencies, are quickly being adopted. ■



▲ *Fig. 10 Attenuation versus frequency of high T_g thermoset and glass microfiber filled PTFE. Data courtesy of Freescale Semiconductor.*



▲ *Fig. 11 Maximum power handling of 5 mil, 50 ohm microstrip lines at 85°C for glass filled PTFE and Astra MT300.*

ACKNOWLEDGMENT

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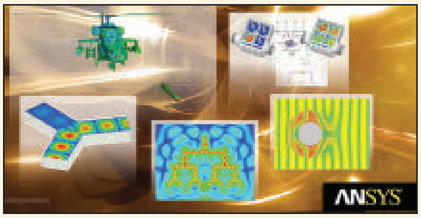
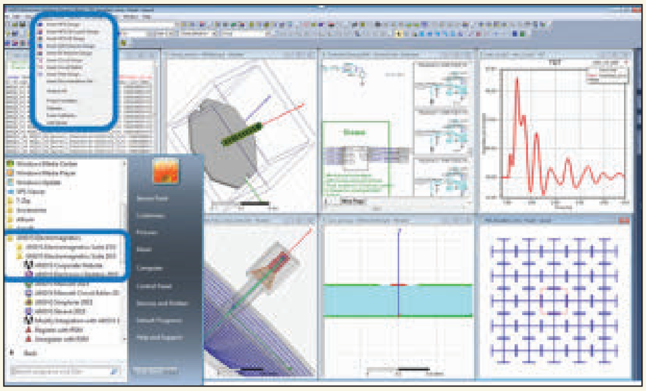
Most Valuable Product



New ANSYS Electronics Desktop Streamlines Wireless Integration

ANSYS
Pittsburgh, Pa.

S-parameters and the network analyzer transformed how RF and microwave engineers share information, enabling them to accurately describe the electrical properties of complicated networks with a simple "black box." This allowed component suppliers and modeling teams to provide comprehensive design information: passive element data (inductors, vias and IC packages) for MMIC/MIC designers and radio blocks (amplifiers, attenuators, filters and couplers) for system integrators. The ability to share device characteristics and protect design IP accelerated the evolution of wireless products and the growth of the supply chain. Today's technology trends and market opportunities require even greater levels of component integration, which call for smaller, lighter, less expensive and wider bandwidth products. These products cannot be represented accurately nor efficiently designed using black boxes that fail to capture their electrical interactions with the surroundings.



▲ *Fig. 1 The ANSYS Electronics Desktop unifies HFSS, Q3D Extractor, HFSS 3D layout, PlanarEM, Circuit and System analysis into a single, unified environment that allows drag-and-drop dynamic links between electromagnetic and circuit simulation.*

To simulate the real world performance of highly integrated devices, designers must account for the electromagnetic (EM) coupling and parasitic behavior resulting from their close proximity to other structures. While high frequency and high speed designers have addressed this with EM simulation, the equivalent of an IP protected, "electromagnetic aware" black box has not existed. In addition, developing tomorrow's wireless electronics requires that multidisciplinary engineering teams share and incorporate physics-based models in larger complex systems, using a collaborative workflow to meet the electrical, thermal and mechanical require-

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OPTIONAL FEATURES:
TIA-422 / TIA 485 Interface • Power Monitoring • Gain Control

FEATURED MILITARY POWER AMPLIFIERS

	MODEL NUMBER	Freq (GHz)	Freq (GHz)	Gain (dB)	Pout (Watts)	PAE (%)	Operation	Voltage (V)	Size (inches)
SATCOM	DM-HPL-35-101	1.625	1.85	20	40	40%	CW	28	4.0 x 4.00 x 1.00
	DM-HPS-35-101	2.2	2.5	20	40	35%	CW	28	4.0 x 4.00 x 1.00
	DM-HPC-60-101	5.5	8.5	50	50	25%	CW	28	2.5 x 2.75 x 0.45
	DM-HPX-100-105	9.75	10.25	50	100	30%	CW	28	7.4 x 4.30 x 1.65
	DM-HPKU-40-105	13.75	14.5	45	50	20%	CW	24	4.5 x 4.00 x 0.78
	DM-HPKU-40-101	14.4	15.5	45	30	15%	CW	28	2.5 x 2.75 x 0.45
	DM-HPKA-10-102	29	31	50	12	15%	CW	20	3.1 x 3.00 x 0.78
	DM-HPKA-20-102	29	31	50	20	15%	CW	20	3.5 x 4.50 x 0.78
RADAR	DM-HPL-1K-101	1.2	1.4	50	1000	40%	100 µs, 10% d.c.	50	6.0 x 6.00 x 1.50
	DM-HPS-1K-102	2.9	3.1	45	1300	35%	100 µs, 10% d.c.	32	14.0 x 8.00 x 1.75
	DM-HPS-1K-103	2.9	3.3	45	1500	35%	100 µs, 10% d.c.	50	9.5 x 9.50 x 1.50
	DM-HPS-1K-104	3.1	3.5	45	1300	35%	100 µs, 10% d.c.	50	9.5 x 9.50 x 1.50
	DM-HPC-50-105	5.2	5.8	50	50	35%	100 µs, 10% d.c.	32	3.0 x 3.00 x 0.60
	DM-HPC-200-101	5.2	5.9	50	200	40%	100 µs, 10% d.c.	50	4.5 x 4.50 x 0.78
	DM-HPX-140-101	7.8	9.6	50	140	40%	100 µs, 10% d.c.	40	3.6 x 3.40 x 0.67
	DM-HPX-400-102	8.8	9.8	50	450	35%	100 µs, 10% d.c.	50	7.0 x 4.50 x 1.65
	DM-HPX-800-102	8.8	9.8	50	900	35%	100 µs, 10% d.c.	50	9.0 x 6.00 x 1.65
	DM-HPX-250-101	9.4	10.1	50	250	40%	100 µs, 10% d.c.	50	3.6 x 3.40 x 0.67
	DM-HPX-800-101	9.4	10.1	50	900	35%	100 µs, 10% d.c.	50	9.0 x 6.00 x 1.65
	DM-HPX-20-101	9.9	10.7	46	20	30%	100 µs, 10% d.c.	32	3.6 x 3.40 x 0.67
	DM-HPX-50-101	9.9	10.7	50	50	30%	100 µs, 10% d.c.	40	3.6 x 3.40 x 0.67
ELECTRONIC WARFARE	DM-HPMB-10-103	0.1	6	55	10	20%	CW	28	2.5 x 2.75 x 0.45
	DM-HPLS-50-101	1	3	50	50	30%	CW	45	4.3 x 3.50 x 0.45
	DM-HPLS-160-101	1	3	16	160	25%	CW	45	6.3 x 6.00 x 0.78
	DM-HPSC-50-101	2	6	50	50	30%	CW	28	2.5 x 2.75 x 0.45
	DM-HPSC-80-101	2	6	50	80	25%	CW	28	4.5 x 4.00 x 0.78
	DM-HPSC-150-101	2	6	60	150	25%	CW	28	6.5 x 6.50 x 0.78
	DM-HPMB-10-101	2	18	45	10	15%	CW	32	2.5 x 2.75 x 0.45
	DM-HPMB-40-101	6	18	50	30	15%	CW	28	2.5 x 2.75 x 0.45
	DM-HPX-25-101	8	11	45	25	30%	CW	28	2.5 x 2.75 x 0.45
	DM-HPX-50-102	8	11	50	50	30%	CW	28	2.5 x 2.75 x 0.45

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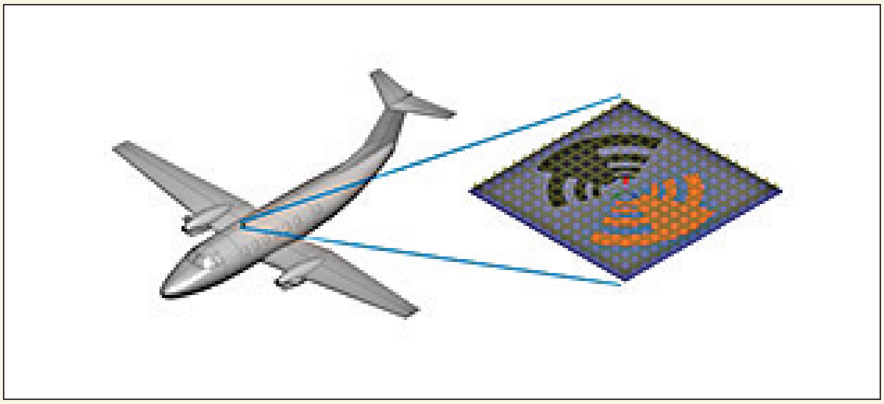


▲ *Fig. 2 A three-layer satellite antenna modeled as a 3D component in ANSYS HFSS. Given the vastly different scales, the antenna is independently meshed from the aircraft platform to efficiently study antenna placement.*

ments. To address all these needs, ANSYS is introducing version 16.0 with the new ANSYS Electronics Desktop featuring ANSYS HFSS and the industry's first 3D EM component library (shown in ***Figure 1***).

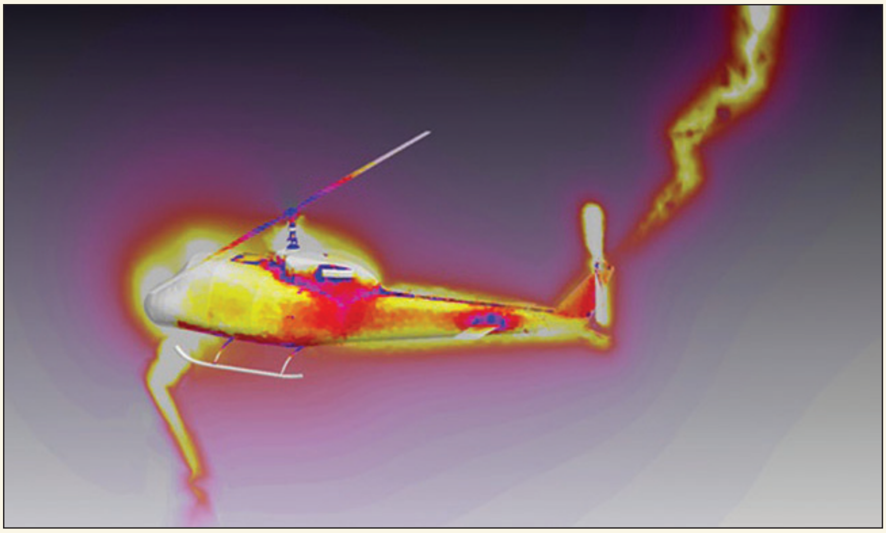
The pending pervasive connectivity of electronic devices (known as the Internet of Things or IoT), compounded by physical design challenges such as through-silicon via (TSV) stacked die and complex multi-chip and multi-package integration (known as more-than-Moore), impose a higher standard for hardware and software reliability. ANSYS 16.0 answers this challenge with a new platform of integrated solver technologies and automation. ANSYS 16.0 meets the increasing demands for electronic reliability and performance, both throughout the design process and across a diverse electronics supply chain.

ELECTRONICS DESKTOP

The new ANSYS Electronics Desktop in version 16.0 is a single environment with a highly integrated interface that provides a streamlined workflow between ANSYS EM field solvers, circuit/system simulators, ECAD links, and EMI/EMC compliance reporting. The integration aids physics-based, first-pass design success. This new platform delivers a single desktop for HFSS, HFSS 3D Layout, HFSS-IE (integral equation solver), Q3D Extractor (quasi-static), Planar EM, Circuit and System simulations. Users can insert HF/SI analysis into coexisting projects with drag-and-drop dynamic links between the EM and circuit simulations. This yields simple problem set-up and reliable performance.

Today's designs are often developed hierarchically from legacy and new building blocks. ANSYS 16.0 introduces the ability to create 3D EM components and integrate them into larger assemblies and systems. These include multi-pin connectors, phased arrays and highly-integrated chip-package-board systems. This capability is especially useful for sharing detailed device models within an organization and between supplier and system integrators. Simulation-ready 3D components can be created and stored in library files, then easily added to larger system designs without needing to apply excitations, boundary conditions and material properties. This leverages the existing information to save engineers valuable set-up time and ensure accurate data entry. All the internal details are incorporated in the original design of the 3D components.

With the wireless industry developing products for the IoT, 5G and commercialized UAVs, there is growing demand for simulation tools that design and integrate devices, antennas, filters and connectors into complex structures such as airframes, appliances, biomedical implants and industrial equipment. ANSYS 16.0 and the new HFSS 3D EM component library target these emerging applications with advanced EM solver technologies and parametric optimization. This enables wireless devices and systems to be simulated from the actual assembly of components and systems. By providing full 3D accuracy to assemblies of varying scale, this latest release accelerates placement studies, ensures



▲ *Fig. 3 New capabilities in the HFSS Transient solver make it easy to simulate time domain scenarios, such as ESD and lightning strikes on aircraft.*

robust design to manufacturing variances and supports collaboration through component sharing.

3D COMPONENT LIBRARIES

The efficient use of the 3D component libraries requires information sharing beyond just geometries. The mesh assembly allows antennas and other parts of the design to be modified without re-meshing the entire structure, which speeds design studies and optimization. For example, IoT designs include antennas placed on equipment, the human body, buildings, base stations and other structures. UAVs have multiple antennas on complex airframes made of composite materials. The 3D component libraries help system integrators solve such complex antenna location problems. ***Figure 2*** shows an example of a thin three-layer antenna, which includes frequency selective surfaces, that can be meshed independently, then placed on the aircraft for efficient placement trade-offs.

The 3D component library models allow encryption to protect collaboration throughout the design chain – potentially an industry changing paradigm. Component modeling with encryption allows users to password protect their component design so that it can be securely shared. Designers can capture the EM interaction between components, which is more accurate than cascading S-parameters and not accounting for the EM interaction. This capability allows specialized designs of antennas and components such as high speed connectors to be used by designers with less experience in RF design.

ADDITIONAL HFSS SOLVER ENHANCEMENTS

ANSYS 16.0 includes several notable enhancements to its HFSS best-in-class EM solver technology. The HFSS Transient option has been upgraded with a new implicit finite element time domain (FETD) technique for simulating time domain scenarios. FETD is especially powerful for electrically small problems, such as lightning strikes on aircraft (as shown in ***Figure 3***), electrostatic discharge (ESD) and time domain reflectometry. The implicit solver provides unconditionally stable time marching, with the time step not limited to the smallest geometric detail. Addressing the challenge of simulating an antenna mounted on a much larger and complex structure, the HFSS-IE solver now includes a powerful multilevel fast multipole method (MLFMM) solver. MLFMM is fast and efficiently uses memory when analyzing problems with extreme electrical dimensions, i.e., more than one hundred wavelengths.

ANSYS 16.0 enhances EM and multiphysics solvers through a new, fully integrated Electronics Desktop with encrypted 3D component libraries. Using these improved tools, RF/microwave designers will be successful addressing the next level of wireless product complexity and system integration.

ANSYS Inc.
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Cliff Drubin, Associate Technical Editor

SABR Will Provide F-16 Pilots with Unprecedented Radar Capability

Northrop Grumman's APG-83 SABR was competitively selected by Lockheed Martin for the F-16 Radar Modernization program to support U.S. and Taiwan Air Force F-16 upgrade programs. Within 16 months of the contract award, the company successfully completed all design reviews and delivered the first engineering, manufacturing and development (EMD) radar to Lockheed Martin. The EMD radar is identical to the production configuration and fully supports the F-16 fleet worldwide.

The company attributes the expeditious development and production of the first EMD radar to the maturity of the system's technology and decades of producing and delivering F-16 radars. "Northrop Grumman's fire control radars have provided vital capabilities for the F-16 and other fighter aircraft for the past four decades," said Jeff Leavitt, vice president, combat avionics systems business unit, Northrop Grumman. "The progress to date in the APG-83 program reflects our enduring commitment to providing American and allied F-16 pilots with significant operational capabilities that give them the advantage for decades to come."

SABR was developed as a multifunction, active electronically scanned array (AESA) fire control radar that provides affordable, reliable fifth-generation air-to-air and air-to-ground radar capability to the F-16. Other AESA fire control radars developed by the company are currently flying on the F-16 Block 60, F-22 Raptor and F-35 Lightning II aircraft.

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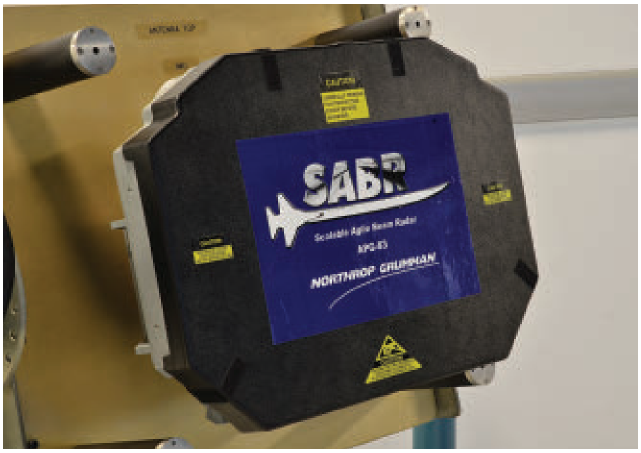

Source: Northrop Grumman Corp.

TriQuint Continues DoD's Trusted Source Status Through 2016

TriQuint Semiconductor Inc. (now Qorvo) announced it has earned continued Trusted Source Category 1A accreditation through 2016 from the Department of Defense (DoD). According to the certification, the accreditation of trust expresses the confidence of the DoD Defense Microelectronics Activity (DMEA) and the National Security Agency's Trusted Access Program Office (TAPO) that TriQuint will continue to deliver trusted foundry microelectronic goods and services (category 1A), which meet the mission critical needs of end users, now and into the future.

TriQuint earned original accreditation for its Richardson, Texas foundry in 2008. It was extended in 2012 to include post processing services, assembly and packaging services and RF test services. All of those accreditations have been renewed through 2016. Foundry accreditations include gallium nitride (GaN), gallium arsenide (GaAs) and bulk acoustic wave (BAW) technologies.

The accreditation certifies that TriQuint provides the DoD and intelligence community with critical system microelectronics, foundry access for mission applications and technology support through industry partnerships. In this manner, TAPO and DMEA can have confidence that national security technology is secured throughout its manufacture and distribution by TriQuint – truly trusted source electronics.

The accreditation certifies that TriQuint provides the DoD and intelligence community with critical system microelectronics, foundry access for mission applications and technology support through industry partnerships.

TriQuint has focused on achieving several milestones as a supplier to the DoD. For instance, the company recently completed the Defense Production Act Title III GaN on silicon carbide (SiC) program. TriQuint also applied the U.S. Air Force Research Laboratory's rigorous manufacturing readiness assessment (MRA) tool and criteria to its GaN production line, which develops high-frequency, high-power devices used within military radar, communications and electronic warfare programs. This MRA process benchmarked TriQuint as the first GaN manufacturer to earn Manufacturing Readiness Level 9, with the maturity needed to support full-rate production programs. The DoD's MRA ensures that manufacturing, production and quality assurance meet operational mission needs and provide the best value for the customer. TriQuint demonstrated that its manufacturing processes met full performance, cost and capacity goals, with the capability in place to support full-rate production.

Raytheon to Implement Modernized ATC System Throughout the National Air Space

Raytheon Co. has been awarded a $350 million Federal Aviation Administration (FAA) contract modification to continue the upgrade of 135 air traffic control centers to the Standard Terminal Automation System (STARS) through September 2017. Implementation of STARS at these airports will bring all of the largest airports and the majority (over 90 percent) of all terminal air space controlled by the FAA onto the NextGen terminal automation platform.

"STARS is now operating at 150 FAA and DoD terminal air traffic control facilities and the performance of the system has been exceptional," said Michael Espinola, managing director, Raytheon Air Traffic Systems. "STARS is the foundation for numerous NextGen efforts within the National Air Space (NAS)."

STARS is implemented under the FAA's Terminal Automation Modernization and Replacement program and brings the terminal automation program into a single operational baseline. This cohesive approach eases the implementation of potential future NextGen initiatives that are designed to maintain safety and bring efficiencies to an increasingly congested NAS.

"STARS is the foundation for numerous NextGen efforts within the National Air Space (NAS)."

STARS is a standard system used by both the FAA and the Department of Defense. It replaces several generations and versions of existing terminal automation systems providing substantial savings in lifecycle costs. The system brings additional safety and capacity management features to terminal automation in both the commercial and defense sectors.

For more than 60 years Raytheon has provided air traffic management technology, products and services to civil and military customers around the world. Raytheon's ATM solutions operate in more than 60 countries and monitor more than 60 percent of the world's airspace.

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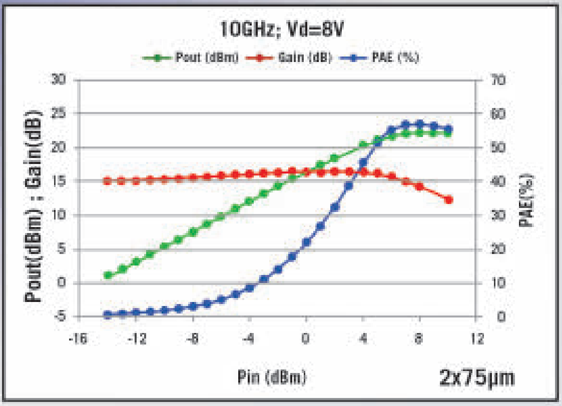
PP25-21 (Class-AB) Tuned for Pout



Gain (dB)	P1dB (dBm)	P1dB (mW/mm)	Psat (dBm)	Psat (mW/mm)	PAE Max(%)
15.0	22.1	1086	22.2	1114	56.8

2x75µm device @8V, 10GHz, 150 mA/mm

Summary of WIN mmWave pHEMT portfolio

	PP25-21	PP15-50/51	PL15-12	PP10-10/11
Gate length	0.25 µm	0.15 µm	0.15 µm	0.1 µm
Max Drain Bias	8 V	6 V	4 V	4 V
Idmax (Vg=0.5V)	490 mA/mm	620 mA/mm	525 mA/mm	760 mA/mm
Peak Gm	410 mS/mm	460 mS/mm	580 mS/mm	725 mS/mm
Vto	-1.15 V	-1.3 V	-0.7 V	-0.95 V
BVGD	20V(18V min)	16V(14V min)	9V(8V min)	10V(8V min)
f_T	65 GHz	90 GHz	100 GHz	130 GHz
f_{max}	190 GHz	185 GHz	150 GHz	180 GHz
Power Density (2x75µm)	1100 mW/mm @ 8V, 10GHz	870 mW/mm @ 6V, 29GHz	580 mW/mm @ 4V, 29GHz	860 mW/mm @ 4V, 29GHz (2x50µm)

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GSA Confirms 360 LTE Networks Launched By End 2014

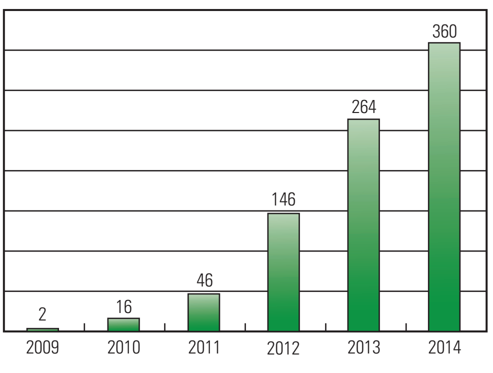
360 operators have commercially launched LTE networks and service in 124 countries, with 96 LTE networks launched in 2014, according to data released by the Global mobile Suppliers Association (GSA) in the latest update of the "Evolution to LTE" report.

The most widely used spectrum for LTE network deployments continues to be 1800 MHz (3GPP Band 3). 158 LTE1800 networks are commercially launched in 76 countries. 1800 MHz is used in almost 44 percent of LTE network deployments and also has the largest user devices ecosystem. Over 42 percent of LTE user terminals can operate in the 1800 MHz band.

The next most popular contiguous band for LTE deployments is 2.6 GHz (Band 7) and is used in over 25 percent of networks. 800 MHz (Band 20) is by far the most popular sub 1 GHz coverage choice for LTE and continued to gain share with almost 1 in 5 operators globally deploying networks using this spectrum.

While most operators deployed LTE networks in paired spectrum using the FDD mode, the LTE TDD mode (TD-LTE) for operators with unpaired spectrum had another year of growth in all regions, especially in China. 48 operators, which equates to more than 1 in 8 LTE operators, have commercially launched LTE service using the TDD mode.

Alan Hadden, president of GSA, said, "LTE-Advanced carrier aggregation deployment was the major trend in 2014. 49 operators have commercially launched LTE-Advanced in 31 countries. Taking account of additional deployments in progress, trials and studies, GSA calculates almost 30 percent of LTE operators are currently investing in LTE-Advanced technology."



Source: GSA's Evolution to LTE report

New ISG on Millimetre Wave Transmission at ETSI

The European Telecommunications Standards Institute (ETSI) has created a new Industry Specification Group (ISG) to work on millimetre wave transmission. The new ISG will facilitate the use of the V-Band (57 to 66 GHz), the E-Band (71 to 76 GHz and 81 to 86 GHz) and in the future, higher frequency bands (up to 300 GHz) for large volume backhaul and fronthaul applications to support mobile network implementation, wireless local loop and any other service benefitting from high speed wireless transmission. The approach is to analyze issues, exchange information and develop common views across the industry on subjects including regulation and licensing schemes, propagation channel models, simulation results, measurements, semiconductor technology roadmaps and experiences gained from early roll-outs and trials.

> The approach is to analyze issues, exchange information and develop common views across the industry...

Other ISG millimetre wave transmission work will focus on use-cases and requirements to identify the most suitable millimetre wave bands for the most important transmission applications. Participation in the millimetre wave transmission Industry Specification Group is open to all ETSI members as well as organizations who are not members, subject to signing ISG Agreements.

NGMN Shares Executive Version of 5G White Paper

The Next Generation Mobile Networks (NGMN) Alliance has published and distributed the executive version of the NGMN 5G white paper. The document provides an initial view on the consolidated operator vision and end-to-end requirements for 5G.

Early in 2014, the NGMN board made the decision to focus the future NGMN activities on defining the end-to-end requirements for 5G in an industry white paper. Since then, more than 100 experts have been working on the definition of these consolidated operator requirements, intended to support the standardization and subsequent availability of 5G for 2020 and beyond.

The NGMN 5G Initiative team has now finalized an executive version of the NGMN 5G white paper, which is published in advance of the full white paper to enable the NGMN partners (leading international operators, vendors and researchers) and other industry stakeholders to consider NGMN's 5G guidelines at this stage. All content areas of the full version are covered in this document provid-

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> The document provides an initial view on the consolidated operator vision and end-to-end requirements for 5G.

ing an initial perspective on the NGMN 5G vision, end-to-end requirements, network design principles and system architecture.

The NGMN Alliance has already established liaisons on 5G with all relevant industry organizations worldwide. In addition, it will work with its partners on the further development and refinement of the final version of the document that will be published at a press conference during Mobile World Congress in March 2015 and will be presented and discussed at the NGMN Industry Conference & Exhibition, March 24-25, 2015 in Frankfurt, Germany.

UK Small and Medium Engineering Firms Funded to Boost Skills

UK small and medium sized engineering firms can now apply for government skills funding to help their businesses grow. The funding forms part of the UK government's work to put employers in the driving seat when it comes to skills and support British engineering to grow and compete.

Engineering companies with fewer than 250 employees will be able to apply for a share of the first £2.5 million of a £10 million match funding pot to develop innovative company-specific training. UK skills minister Nick Boles said, "A company's greatest asset is its people and making sure they have the right skills is vital in supporting the long-term economic plan. This funding gives employers the power to unlock the full potential of their workforce by designing and developing training catered to their specific needs. I encourage all small and medium sized engineering firms to consider how they could use this funding to take their business to the next level."

The new fund forms part of a £30 million initiative that sees government and employers join together to invest in engineering skills. It was announced as a response to Professor Perkins' review of engineering skills. The first two tranches of funding were targeted at improving engineering careers and developing women engineers. The final tranche is specifically designed with small and medium sized businesses in mind.

Tim Thomas, head of skills and employment policy at EEF said, "We are delighted that this scheme has now been opened to SME employers and that the minimum grant, which a company would need to match with their own money, has been dropped to £10,000. This makes the scheme far more accessible and realistically reflects the amount many smaller companies may be able to invest in skills and training.

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Model	Power Measurement	Frequency MHz	Control Interface	Price $ ea. (Qty 1-4)
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PWR-4GHS	Peak	0.009 to 4000	USB	795.00
PWR-6GHS	Peak	1 to 6000	USB	695.00
PWR-8GHS	Peak	1 to 8000	USB	869.00
NEW! PWR-8GHS-RC	Peak	1 to 8000	USB & Ethernet	969.00
PWR-8FS	Peak	1 to 8000	USB	969.00
PWR-4RMS	Average	50 to 4000	USB	1169.00

*Measurement speed as fast as 10 ms for model PWR-8-FS. All other models as fast as 30 ms.

†Dynamic range as wide as -35 to +20 dBm for model PWR-4RMS. All other models as wide as -30 to +20 dBm.
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Cliff Drubin, Associate Technical Editor

5G in 2020 Will Be Rare; Over 100 Million Subscribers by 2025

VIEW VIDEO

According to new market data forecasts from ABI research, it will take more than five years for 5G to reach the 100 million subscriber mark—two years longer than 4G. 4G subscriber growth was much faster than with previous generations, fueled by the capabilities of increasingly powerful smartphones and the availability of 4G devices. 5G subscriber growth will likely be a bit more muted at first due to the increased complexity of 5G cells and networks, but will pick up in 2023.

"There are a number of commonalities between countries that are early builders of 5G networks. They have a large population, of which a large percentage is living in urban areas. They also have many companies pushing the envelope with IoT strategies. These countries will drive 5G subscriber volumes," said ABI research director, Philip Solis. "They are the United States, China, Japan, South Korea and the United Kingdom in order of 5G subscribers in 2025."

It is also important to understand the nuances around 5G to recognize where it is headed. "5G will be a spectrum of evolution to revolution—it will be an evolution of the way the core network and network topology is transforming now, but it will be clearly delineated as a fifth generation mobile air interface on which the mobile network of the 2020s and 2030s will be built," added Solis.

> "5G will be a spectrum of evolution to revolution ..."

5G will encompass spatial division as the foundation of the air interface, leveraging techniques like massive MIMO—achievable in devices because of the high frequency of spectrum that will be used—and 3D beam forming to form narrow beams that divide the space around a 5G base station. Client devices will have links to multiple cells simultaneously for robust connectivity. Spectrum will be used flexibly and shift as needed between access and fronthaul and backhaul. The waveform and modulation scheme are the least clear aspects of 5G currently.

A 5G network will be a network of small cells and will be practical in urban and industrialized environments for the population density and the reflections in urban canyons; however, expect a scaled down version of 5G to use existing spectrum for macrocells as well in the longer term. One potentially problematic issue, however, will be regulatory issues concerning concentrated RF beams in centimeter and millimeter wave spectrum.

Indoor Location Deployments on Course to Hit 25,000

It has been a breakthrough year for indoor location for retail, with ABI Research's quarterly indoor location technology tracker forecasting deployments to approach 25,000 by the end of 2014, up more than 100 percent from 2013.

Senior analyst Patrick Connolly commented, "Vertically, the bulk of deployments are in clothing, big box, grocery and shopping malls in 2014, driven by a variety of applications such as customer analytics, offers/coupons, product search, staff management and navigation. Looking into 2015, we can expect to see the quick serve restaurant (QSR) market growing with a significant demand for queue management technologies as illustrated by companies like Starbucks and Taco Bell which launched queue-skipping smartphone applications in 2014."

"What is interesting is the technology mix today. We are seeing growth across all major technologies, including BLE, Wi-Fi and audio, with 2015 being an important year for handset-based location, sensor fusion, magnetic field and LED. Regionally, the focus is very much on the United States in 2014 but there are now many worldwide deployments. This is a market where we expect to see concurrent growth across the globe with a slew of regional and vertical winners, rather than one company dominating the whole space," added Connolly.

> "...the bulk of deployments are in clothing, big box, grocery and shopping malls in 2014, driven by a variety of applications such as customer analytics, offers/coupons, product search, staff management and navigation..."

Looking at market share — shopkick/SK Telecom, Point Inside and Aisle411 are now leading in deployments. Over the past 12 months there has been a considerable change in deployments as companies have moved from a handful of deployments to getting into the hundreds and thousands of stores. In 2015, we also expect to see camera analytics companies like ShopperTrak, Irisys and Brickstream playing an increasing role as they expand their offering into BLE, Wi-Fi and in-store analytics—expect to see a lot of announcements around this at NRF 2015 as these companies launch new technologies and partnerships.

Small Unmanned Arial Systems Market to Exceed $8.4B by 2019, Dominated by Commercial Sector

The small unmanned arial systems (sUAS) market will surpass $8.4 billion by 2018 according to new research published by ABI Research entitled "Small Unmanned Aerial Systems (sUAS) Solutions Ecosystem." By 2019 the commercial sector will dominate the overall sUAS market with revenues exceeding $5.1 billion (51% 2014 to 2019 CAGR), roughly 5× larger than the prosumer/hobby market, and 2.3× greater than the military/civil

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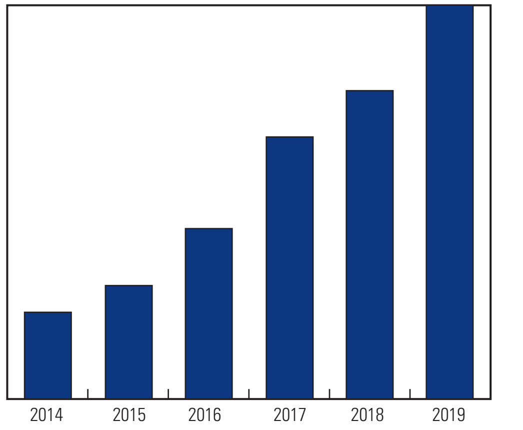
> "The commercial sector is the sweet spot for the sUAS market, a fact recognized by both traditional defense industry suppliers..."

market segment. Moreover, it is application services—industry specific applications, as well as data, operator and modeling services—and not platforms and other hardware technologies, which will be the key driver for the growth of the commercial sector.

Ongoing research advancements, technological developments, and rapidly dropping prices for increasingly capable enabling technologies, have combined to remove barriers to innovation and commercialization, and spur the development of new sUAS and increase the ways they can be applied. For this study, the sUAS market was not defined by, or limited to, the unmanned aerial system platforms and airframes alone, but also includes other technologies, products and services that are ancillary to, and often necessary for the use of small unmanned vehicles, along with the many applications enabled by them.

According to Dan Kara, practice director, robotics at ABI Research, "The commercial sector is the sweet spot for the sUAS market, a fact recognized by both traditional defense industry suppliers such as Elbit Technologies, AeroVironment and Aeryon Labs, as well as providers to the prosumer/hobbyist marketplace including DJI, Parrot, SenseFly, 3D Robotics and others. As a result, both groups of sUAS makers, along with other classes of solution providers, are aggressively targeting the commercial sector through acquisitions, internal development, partnerships and investment.

Commercial sUAS Platform Revenue
World Market Forecast: 2014 to 2019



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Around the **Circuit**

Barbara Walsh, Multimedia Staff Editor

MERGERS & ACQUISITIONS

RF Micro Devices Inc. and **TriQuint Semiconductor Inc.** announced they have completed their merger of equals to form **Qorvo™**, a new leader in RF solutions. As a result of the merger, which is intended to qualify as a tax-free reorganization, TriQuint shareholders will receive 1.675 shares of Qorvo and RFMD shareholders will receive 1 share of Qorvo for each TriQuint or RFMD share held, and a one-for-four reverse stock split was effected at closing. Former shareholders of RFMD and TriQuint will each own approximately 50 percent of Qorvo.

Rogers Corp. announced it has signed a definitive agreement to acquire **Arlon LLC**, currently owned by Handy & Harman Ltd., for $157 million, subject to closing and post-closing adjustments. The transaction is expected to close in the first half of 2015. Rogers intends to finance the transaction through a combination of cash and borrowings under an existing bank credit facility. The proposed acquisition of Arlon is consistent with Rogers' strategy as it adds complementary solutions to its printed circuit materials and high performance foams business segments and expands the company's capabilities to serve a broader range of markets and application areas.

COLLABORATIONS

L-3 Southern California Microwave announced that it has been selected by **Lockheed Martin's Mission Systems and Training** business to provide its MICRO Secure Digital Data Link as the secure command & control and ISR communications backbone for the UK Ministry of Defence's (MoD) digital Desert Hawk III DDL small unmanned aircraft system (SUAS) platform. The MICRO SDDL transceivers enable optimal utilization of frequency spectrum through a single RF channel supporting an IP-based, bidirectional TDMA secure communications link.

Molex Inc., a global manufacturer of electronic solutions, announced it has signed a definitive agreement as a strategic partner and investor in Chicago-based **NuCurrent**, a developer of wireless power antenna technology. NuCurrent created a breakthrough in structures for low resistance antennas, initially for the medical device market. It now offers custom design and fabrication of high efficiency inductors geared toward specific functions with a growing focus on wireless power applications in the consumer sector.

TowerJazz announced that **Fairchild Semiconductor** has started mass production at TowerJazz Panasonic Semiconductor Co.'s (TPSCo) fabrication facility in Tonami, Japan. This is a process transfer from Fairchild of its state of the art discrete devices for the industrial and consumer markets. This development has been in the works for several months involving significant transition efforts between Fairchild and TowerJazz. TowerJazz's TOPS business model enables its customers to transfer the company's process flows into TowerJazz's worldwide manufacturing facilities, providing them with needed capacity, manufacturing flexibility and competitive cost.

ACHIEVEMENTS

Rice University is offering engineering students a unique opportunity to show potential employers that they are graduating with the right stuff to lead. In May, Rice will begin awarding a Certificate in Engineering Leadership to graduates who complete an internship, 10 credit hours of required courses and labs, a portfolio and final presentation. The program, the first of its kind in Texas and one of just a handful in the United States, is offered through the Rice Center for Engineering Leadership.

Satellites may soon carry Raytheon's GaN technology into Earth's orbit. **Raytheon Co.** has successfully validated its GaN MMIC technology for use in space-bound equipment. Raytheon GaN MMICs, fabricated at its Andover, Mass. foundry, demonstrated the radiation hardness required for space through single event burn-out (SEB) and total ionizing dose (TID) testing. The results showed the devices are not susceptible to catastrophic failure caused by heavy ions. Further testing showed no loss of performance at exposure levels up to 1 Mrad, significantly more than is needed for typical space applications.

Alvarion Technologies announced that its BreezeULTRA P6000 was awarded certification by the internationally recognized MiCOM Labs for Japan's Technical Regulations Conformity Certification of specified radio equipment. Alvarion Technologies claims to bring the highest capacity product in the wireless broadband point-top-point, license-exempt market along with high density events and smart city solutions. Offering a bold combination of capacity, performance, organic growth and ease of use capabilities, Alvarion Technologies enjoys a global presence in their solutions with over 25,000 sites in 95 countries.

CONTRACTS

Engility Holdings Inc. announced it has won a $61 million single award indefinite-delivery/indefinite-quantity (IDIQ) contract to provide engineering services and related research, development, test and evaluation efforts in support of the Naval Air Warfare Center Weapons Division (NAWCWD). Under this award, Engility will provide a range of engineering services for the functional organizations that support numerous Department of Defense (DoD) weapons acquisition programs.

Harris Corp. has been awarded a three-year, $20 million contract by the National Oceanic and Atmospheric Administration (NOAA) for the Geostationary Weather Satellite Antenna System program. The contract was awarded in the first quarter of Harris' fiscal year 2015. Harris will provide its new WxConnect™ products that receive and process satellite weather observations from the NOAA Geostationary Operational Environmental Satellite R-Series Re-

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broadcast (GRB) and Japanese HimawariCast services. These products will be deployed at eight National Weather Service locations to support a broad range of mission critical forecasting operations.

Exelis has been awarded a $10.3 million sole source U.S. Air Force contract to insert a modern data storage and retrieval technology into the Strategic Automated Command Control System (SACCS). The SACCS provides orders and pass codes authentication for Air Force nuclear weapons platforms, bombers and support units. Inserting a modern data storage system into this command and control system will dramatically improve retrieval and verification of critical data for decision-makers. The upgrade by Exelis, a provider of critical network solutions, will also allow the existing system to continue with uninterrupted service through 2030.

Comtech Telecommunications Corp. announced that its Orlando, Florida-based subsidiary, Comtech Systems Inc., has received $7.4 million in contract add-ons for a satellite system project for end-use by the Brazilian Military. These orders, the substantial majority of which were received in November 2014, consist of additional satellite terminal designs and the supply of equipment and services to implement the project.

Mercury Systems Inc. announced it has received a $2.6 million purchase order relating to a sensor processing application for fighter aircraft. The order was booked in the company's fiscal 2015 second quarter.

Northrop Grumman Corp. has been selected by prime contractor **Lockheed Martin** to provide its space inertial reference system for the U.S. Air Force Space-Based Infrared System's (SBIRS) fifth Geosynchronous Earth Orbit (GEO) satellite. Northrop Grumman will provide its Scalable Space Inertial Reference Unit (Scalable SIRU™) for sensor pointing/stabilization and attitude control on the SBIRS GEO-5 mission. Northrop Grumman has also provided its Scalable SIRU for previous SBIRS GEO satellites. The SBIRS program delivers early warning of ballistic missile launches, missile defense, technical intelligence and battle space awareness.

The French defense procurement agency, Direction Générale de l'Armement (DGA), has awarded a contract to **ThalesRaytheonSystems** to supply the French armed forces with 12 fixed Ground Master 400 radars and four mobile tactical Ground Master 200 radars. The radar systems supplied are designed to protect key assets to forces deployed in remote operations and are able to detect modern threats, such as unmanned aircraft vehicles (UAV), from a wide range of altitudes. The systems will also be coupled with the NATO Air Command and Control system to provide airspace monitoring and ground-based air defense detection.

PEOPLE

Keysight Technologies Inc. announced that **Gregg Peters**, vice president and general manager, Keysight

We've been traveling safely at speeds up to 79 GHz for many years

Circuit boards are being pushed harder, with frequencies for automotive radar systems and mobile backhaul communications links climbing to 79 GHz and beyond. Just as designers of satellite communication systems have for decades, now designers of these commercial applications are counting on the circuit boards and materials used within them for consistent, reliable operation at millimeter wave frequencies. History proves that Circuit Materials from Rogers Corporation are the ideal choice.

Whether they are based on Rogers RO4835™ LoPro™ circuit materials or RO3003™ laminates, these higher-frequency applications depend on reliable substrates with consistent performance in the 79 GHz range. Both RO4835 LoPro and RO3003 circuit materials feature best in class electrical performance across diverse environments including a wide temperature range and elevated humidity.

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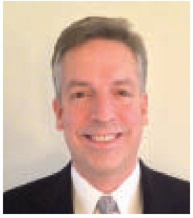
Around the **Circuit**

▲ *Gregg Peters*

Component Test Division, was recently appointed as the first chairman of the Electrical and Computer Engineering Department Heads Association (ECEDHA) Corporate Advisory Council (CAC). ECEDHA is composed of heads and chairs of departments offering accredited programs in electrical and/or computer engineering and includes members from almost 90 percent of all qualified U.S. university programs. The CAC serves as the principle liaison between the council and the ECEDHA board of directors providing industry feedback and valuable recommendations.



▲ *Jay Colognori*

Zentech Manufacturing Inc. announced that **Jay Colognori** has joined the team as director, business development/mil-aero and space markets. Colognori is widely respected in the Mid-Atlantic market and beyond for driving innovative engineering solutions to solve the most challenging of printed circuit board requirements. His prior positions include sales engineer/strategic account roles with both DDI and Viasystems. His primary responsibility will be leading Zentech's growth initiatives in the mil-aero and space markets nationwide and leveraging Zentech's position as the first electronics contract manufacturer certified to the IPC J-STD 001 Space Addendum Qualified Manufacturer List (QML).

▲ *Christian Grieswelle*

RFMW Ltd. announced that **Christian Grieswelle** has been promoted to the position of director of sales for RFMW Europe. Grieswelle has served as RFMW's Germany country manager for the past three years. As such, he has established a successful track record of developing RFMW's presence in Germany. In recognition of Grieswelle's business development and keen managerial skills, he will be leading and further developing the European sales team who now report to him in their entirety. Grieswelle graduated with a degree in electrical engineering from the University of Paderborn, Germany.

▲ *Vince Wright*

Richardson RFPD announced that **Vince Wright** has joined the company's sales team. He will focus on the RF and wireless market as a technical sales engineer, supporting customers in Maryland and reporting to Mike Fraser. Prior to joining Richardson RFPD, Wright was the national sales manager for Reactel Inc., in Gaithersburg, Md., where he worked with major defense contractors as well as commercial wireless and CATV providers.

Raytheon Co. chairman and CEO Thomas A. Kennedy announced the appointment of **David C. Wajsgras** as

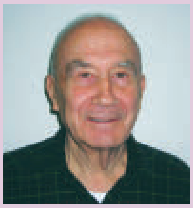
Around the **Circuit**

▲ *David C. Wajsgras*

president, Raytheon Intelligence, Information and Services (IIS) business, succeeding Lynn A. Dugle, who has announced plans to retire from the company. Kennedy has appointed **Anthony F. "Toby" O'Brien** as vice president and chief financial officer, succeeding Wajsgras. The new appointments are effective March 2, 2015.

TMD Technologies Ltd., a manufacturing SME in the defense industry, has appointed **Tracey Lofts** to the new board level position of engineering and programmes director. Lofts has worked at TMD for five years in the role of divisional manager. In her new position, Lofts will provide leadership for TMD's engineering and programme management with particular objectives centered around schedule, budget and innovation.

IN MEMORIAM



Dan Massé passed away on January 10 after a long illness at the age of 85. Originally from Provins, France, Dan came to the U.S. in 1957 and eventually settled in Walpole, Mass. He was an engineering manager at Raytheon Co. and editor of *MTT Transactions* prior to joining *Microwave Journal* in the early 2000s. Dan spent 12 years serving as MWJ's associate technical editor, ensuring the scientific merit of our technical content. He was also lead editor of our monthly commercial and defense reports. Dan is survived by his beloved wife of 56 years, Thelma Massé, two daughters and two grandchildren.

REP APPOINTMENT

Insulated Wire Inc., Microwave Products Division announced a new distribution agreement with **HASCO Inc.** for the Re-Flex™ product range. Re-Flex™ is widely used for both systems and test equipment applications where the ability to make tight bends is a consideration, and multiple bending does not cause the micro fracturing and leakage issues experienced with other hand formable cables. HASCO Inc. has stock available for immediate delivery of RF141 (RG402 line size) assemblies in a range of lengths starting at 2" with both direct solder and shell style SMA connectors, operating to 18 and 26.5 GHz respectively.

PLACES

Horizon House Publications and ***Microwave Journal China*** announced that EDI CON 2015, taking place April 14-16, has added a 5G Advanced Communications Forum to the conference schedule. The 5G Forum will be a full day of sessions taking place on April 15 at the China National Convention Center (CNCC). The 5G Forum will kick off with China Mobile presenting their perspective on 5G technologies followed by a panel session including experts from organizations such as China Mobile, Shanghai Tech, Keysight Technologies, Rohde & Schwarz and National Instruments.

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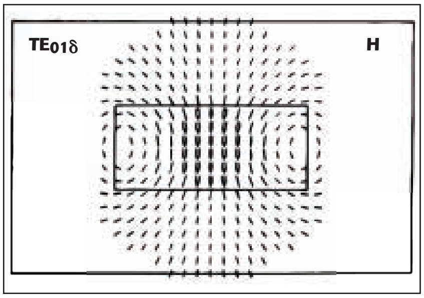
INVITED PAPER

An Overview of High Q TE Mode Dielectric Resonators and Applications

Edward C. Liang
MCV Microwave, San Diego, Calif.

The widespread use of ceramic dielectric resonators in place of metallic resonant cavities in RF and microwave circuits started in the 1970s, with the first low loss, temperature stable barium tetratitanate ceramic materials.[1] Further development of high dielectric constant ceramics with adjustable temperature coefficients enabled microwave engineers to use these materials in oscillator and narrowband filter designs for radar detectors, cellular phone and public safety base stations, satellite receivers and satellite broadcasting (TVRO/DBS) applications.

The most direct way of reducing the cost of microwave circuits is by reducing their size. The size of a dielectric resonator is considerably smaller than that of an air resonant cavity at the same frequency, because the relative dielectric constant of the material is substantially larger than unity, the dielectric constant of air. The resulting size reduction approximately equals the square root of the resonator's dielectric constant, $\sqrt{\varepsilon_r}$. For example, a resonant circuit using a dielectric resonator with $\varepsilon_r = 38$ will be more than six times smaller than the equivalent air resonant cavity.



▲ *Fig. 1 Magnetic field of* $TE_{01\delta}$ *isolated dielectric resonator.*

TE MODE RESONATORS

A dielectric resonator can be a short solid puck, cylindrical, tubular, spherical or even a parallelepiped shape. A commonly used resonant mode in cylindrical dielectric resonators is $TE_{01\delta}$. The magnetic field or dipole is shown in ***Figure 1***, and the electric field consists of simple circles concentric with the axis of the cylinder is shown in ***Figure 2***. Because of the high relative dielectric constant, a typical dielectric resonator stores more than 95 percent of its electric energy and over 60 percent of its magnetic energy in the $TE_{01\delta}$ mode inside the cylinder. The remaining magnetic energy in the air around the cylinder decays rapidly with distance away from the resonator surface.

Choosing the ratio of the length of the resonator to its diameter to be in the range of 0.35 to 0.45 is most favorable because the fundamental resonant mode, $TE_{01\delta}$, exhibits a large enough frequency separation from other spurious modes, such as $TM_{01\delta}$.[2] Mode separation can be accentuated by incorporating a con-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centric bore in the resonator cylinder where the electric field is weakest.

To a first order, the diameter of a cylindrical TE mode resonator at a resonant frequency F_0 is given by

$$D_r = \frac{c}{F_0\sqrt{\varepsilon_r}} \qquad (1)$$

where D_r is the diameter of the resonator, ε_r is the dielectric constant of the resonator and c is the velocity of light. This assumes $D_r \sim 2L_r$, where L_r is the length of the resonator.

Although the resonant frequency of a dielectric resonator can be computed exactly by solving Maxwell's equations, it is considerably more complex to compute the resonant frequency for a dielectric resonator mounted on microstrip or placed within a shielded metal cavity. The metal wall can affect the magnetic field and contributes to metal loss. When $0.35\ D_r \le L_r \le 0.45\ D_r$, the resonant frequency F_0 (in GHz) of an isolated dielectric resonator in $TE_{01\delta}$ mode can be calculated by

$$F_0 = \frac{233}{\sqrt{\varepsilon_r}^{\,3}(V)^{1/3}} \qquad (2)$$

where V is the volume of the dielectric resonator

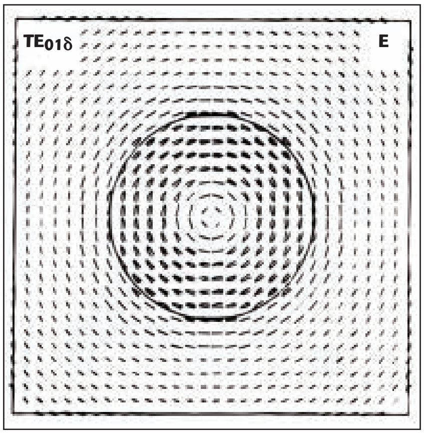
$$V = \left(\frac{\pi D_r^2 L_r}{4}\right)$$

D_r is the diameter of the dielectric resonator (in mm), and L_r is the length of the resonator (in mm).

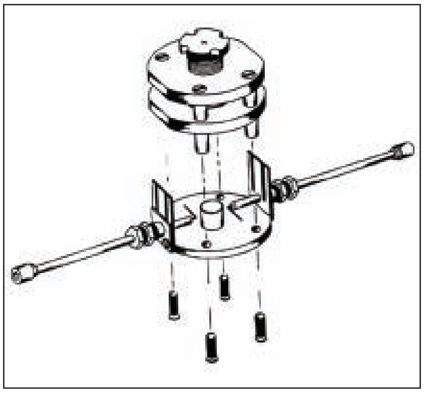
The dielectric constant of the resonator can be measured to within 0.3 percent by using the parallel-plate procedure first introduced by Hakki and Coleman,[3] assuming dimensional accuracies within ± 0.5 mils (± 127 μm) and frequency within ± 1 MHz. This method was later investigated for error analysis and temperature effects and is now commonly known as the Courtney method.[4] ***Figure 3*** shows the test fixture used for the measurements.

CIRCUIT INTEGRATION

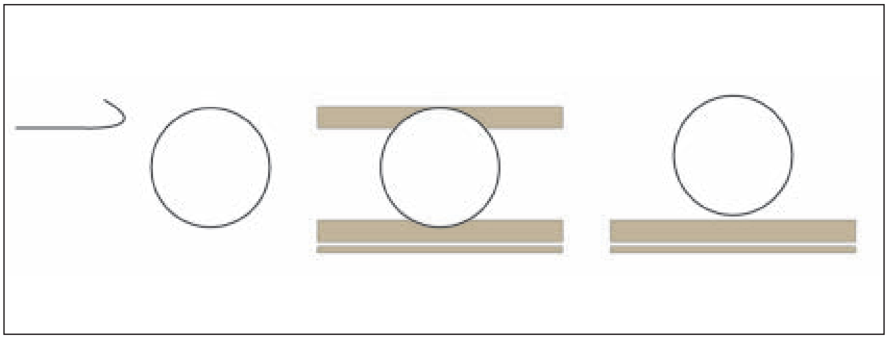
$TE_{01\delta}$ mode dielectric resonators are generally magnetically coupled to the surrounding circuits. The most



▲ *Fig. 2 Electric field of $TE_{01\delta}$ isolated dielectric resonator.*



▲ *Fig. 3 The Courtney holder for measuring dielectric constant.*

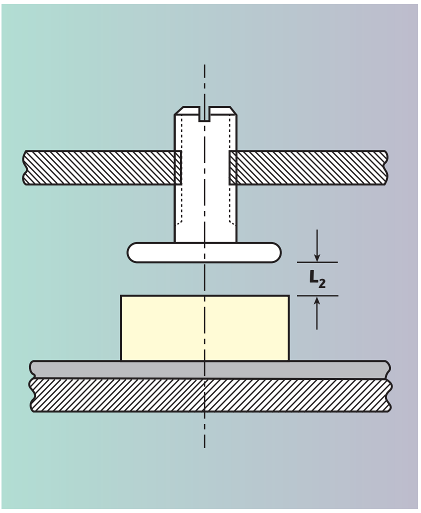


▲ *Fig. 4 Methods for coupling to the dielectric resonator.*

effective methods are bent coaxial probes or microstrip lines, as shown in ***Figure 4***.

Metal cavities are usually used with resonator circuits because very high Q factors and accompanying narrow bandwidths can be obtained, and electromagnetic fields can be sustained within a lossless cavity at the resonant frequency. To eliminate conductor losses and environmental effects, shielding walls are best positioned away from the dielectric resonator, at a distance at least the radius of the resonator.

When a metal wall of a cavity is moved inward, the resonant frequency of the resonator will either decrease or increase, depending on whether the stored energy of the displaced field is predominantly electric or magnetic, respectively. Therefore, the resonant frequency must be fine-tuned. A screw mounted metal or dielectric plate can be used, or alternatively, a solid ceramic cylinder can be moved up and down between the shield cover wall and the dielectric resonator (see ***Figure 5***). The gap created between the tuner and dielectric resonator (L_2 in Figure 5) perturbs the fringe electromagnetic fields that exist outside the dielectric resonator. A metallic tuner approaching the dielectric resonator increases F_0, and a dielectric tuner decreases F_0. Up to 20 percent tuning can be achieved; however when using a metal tuner, the tuning range should be limited to only a few percent to avoid seriously degrading the Q factor and affecting the temperature coefficient of the dielectric resonator. The objective is to



▲ *Fig. 5 Tuning the frequency.*

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tune F_0 while maintaining the same Q factor and temperature coefficient.

Typically, the outer and inner diameters of the dielectric resonator are kept constant within machining tolerances, and the length or thickness of the resonator is adjusted to compensate for small lot-to-lot and piece-to-piece F_0 variations. Changing the diameter of the resonator or removing small quantities of ceramic from the resonator enable extremely tight F_0 tolerances to be achieved, from ± 0.05 to ± 0.5 percent. A large resonator can be fine-tuned by attaching small tuning chips or pieces of ceramic material to the resonator using a low loss adhesive. The F_0 can be lowered incrementally by adding various sizes or varying the position of the tuning chips; this approach achieves a tuning range of -1 to 2 percent.

QUALITY FACTOR

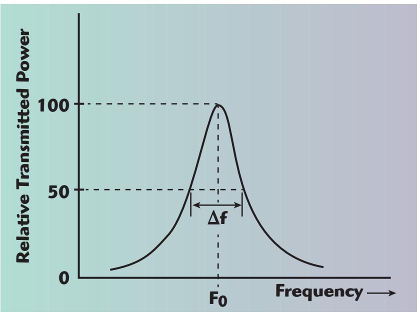
The figure of merit for assessing the performance or quality of a resonator is the quality factor, Q, which is a measure of the energy loss or dissipation per cycle compared to the energy stored in the fields of the resonator. The Q factor is defined by

$$Q = 2\pi \frac{\text{maximum energy storage during a cycle}}{\text{average energy dissipated per cycle}} \quad (3)$$

$$= \frac{\omega_0 W_0}{P} = \frac{2\pi W_0}{PT} \quad (4)$$

where W_0 is the stored energy, P is the power dissipation, ω_0 is the resonant radian frequency and T is the period $(2\pi/\omega_0)$. With a typical frequency response as shown in ***Figure 6***, to a very good approximation, the loaded quality factor, Q_L, in a transmission curve is given by,

$$Q_L = \frac{\omega_0}{\Delta\omega} = \frac{F_0}{\Delta f} \quad (5)$$



▲ *Fig. 6 Relative transmission power as a function of frequency.*

A cavity or resonator must deliver power to an external load in order to be useful.[5] The loaded quality factor, Q_L, defines the overall power loss in a cavity or resonator system and includes both internal and external losses. The unloaded quality factor, Q_u, accounts for the internal losses, and the external quality factor, Q_e, accounts for external losses. The relationship between Q_e, Q_u and Q_L is given by

$$\frac{1}{Q_L} = \frac{1}{Q_e} + \frac{1}{Q_u} \quad (6)$$

This shows that the smallest quality factor dominates. Hence, engineers using low loss dielectrics must consider the conductor and cavity structures to preserve the loaded Q factor in actual systems.

Q_u is typically measured in a test cavity with dimensions that are at least two to three times the size of the dielectric resonator, to simulate an isolated and shielded resonator. A low loss, low ε_r material is used to support the resonator in the center of the fixture, and a bent coaxial probe is used for signal coupling. By employing such a test fixture with a dielectric resonator aspect ratio (L_r/D_r) in the range of 0.35 to 0.45, the F_0, 3 dB bandwidth (Δf) and insertion loss (IL) can be measured using a network analyzer. Q_u is then calculated using the equation

$$Q_u = \frac{F_0}{\Delta f} / \left(1 - 10^{-IL/20}\right) \quad (7)$$

By eliminating the external loss Q_e from the metal shielded wall, Q_u just equals the dielectric resonator quality factor, Q_d. Actual microwave circuits may have cavity dimensions only two times the size of the dielectric resonator or smaller. If the side wall or metal shield is close enough to the resonator, the TE resonant frequency will be affected by the size of the cavity and external loss will contribute to Q_u. Including all contributors, the overall quality factor can be expressed as

$$\frac{1}{Q_L} = \frac{1}{Q_d} + \frac{1}{Q_c} + \frac{1}{Q_r} + \frac{1}{Q_e} \quad (8)$$

where Q_d is the quality factor of the dielectric resonator, Q_c is the contribution from the metal wall, and Q_r reflects losses from radiation. The first three terms on the right hand side of the equation make up the unloaded Q_u factor of the resonant cavity:

$$\frac{1}{Q_u} = \frac{1}{Q_d} + \frac{1}{Q_c} + \frac{1}{Q_r} \quad (9)$$

When the shield is entirely closed and there is no radiation loss, the third term can be ignored.

▲ *Fig. 7 Custom resonator test cavities.*

Because conductor loss from the Courtney holder may contribute to the loss tangent (tan δ) measurement, some have estimated ± 40 percent error in tan δ. Kobayashi and Katoh[6] proposed a clever way to remove the effect of conductor loss by using two different resonant modes, TE_{011} and TE_{01p}, to obtain a much more accurate measurement. With a test cavity whose size is greater than twice the dielectric resonator and where the parallel plates are less than a half wavelength of air $(\lambda_0/2)$, the conductor and radiation

loss terms can generally be removed. Then the unloaded Q factor is approximately equal to the dielectric Q factor, or $Q_u = Q_d$.

TEMPERATURE EFFECTS

The first temperature effect on the dielectric resonator is from thermal expansion, which is generally a small positive number. The physical dimensions increase with increasing temperature, resulting in a constant thermal coefficient of expansion, α, measured in ppm/°C. The relative dielectric constant, ε_r, also varies with temperature. As a first approximation, the change in ε_r is linearly proportional to temperature and can be represented by a constant, denoted by τ_ε.

Therefore, the resonant frequency of a dielectric resonator will change with temperature from both the linear thermal expansion and the change in dielectric constant. The sensitivity of the resonant frequency to temperature changes, known as the temperature coefficient of resonant frequency, is given by the expression

$$\tau_f = \frac{\Delta f}{f \Delta T} \tag{10}$$

By taking the appropriate derivatives of equation 10, we obtain

$$\tau_f = -\alpha - \frac{\tau_\varepsilon}{2} \tag{11}$$

For cavities filled with inhomogeneous materials, equation 11 is modified to include a filling factor, P_e, to account for the surrounding environment.

$$\tau_f = -\alpha - \frac{\tau_\varepsilon}{2} P_e \tag{12}$$

P_e can be very close to unity for homogeneous cavities and less than unity for inhomogeneous cavities.

Depending upon the size and proximity of the cavity to the dielectric resonator, the thermal expansion of the cavity may contribute a substantial amount to the temperature coefficient of the dielectric constant τ_ε, leading to a discrepancy between the calculations and the actual τ_ε in the design.[7] For best results, τ_ε should be measured, generally between 20 and 120°C is sufficient to determine the linear relationship.

COMMERCIAL HIGH Q DIELECTRIC RESONATOR MATERIALS

Early resonators with dielectric constants near 36 were based on barium polytitanates and Zr(Ti,Sn)O_4. Ultimately, resonators evolved to higher Q, low τ_f crystalline phases having more complex chemistries, fabricated with materials in the $BaO - TiO_2 - ZnO - Nb_2O_5/Ta_2O_5$ and $ZrO_2 - TiO_2 - ZnO - Nb_2O_5$ systems. Perovskite compounds incorporating Nd_2O_3, TiO_2 and CaO/SrO or BaO, ZnO, CoO and Nb_2O_5 are also used.[8] Such resonators have dielectric constants from 34 to 47 and with typical $Q \times f_0$ values of 40,000 to 70,000, when measured between 5 and 6 GHz.

Super high Q resonators with dielectric constants near 30 and 24 are now commercially available. Ultra high $Q \times f_0$ values range from 100,000 to 300,000 can be obtained when measured near 10 GHz. These are based

on perovskite compounds incorporating BaO, MgO, ZnO and Ta_2O_5, with additives to control and vary τ_f. These super high Q resonators are primarily used for dielectric resonator oscillators (DRO) at K_u and K-Band. Precise mechanical dimensions and very tight tolerance in ε_r (± 0.5) and τ_f (0.5 percent) are required for K-Band DRO applications. Unlike the first group of dielectric resonators, to maintain the extremely tight tolerances in electrical properties and Q values, super high Q resonators require much more experience in dielectric materials research and development as well as expertise in powder processing and manufacturing technology.

CONCLUSION

Successful utilization of high Q dielectric resonators in resonant cavities relies on precision control of the raw materials, recipes, powder processing, manufacturing and custom adjustment in actual applications. Consistent lot-to-lot and piece-to-piece resonator performance ensures successful designs and high yield production. Understanding how boundary conditions affect the resonant frequency, dielectric constant, quality factor and the temperature coefficient of resonant frequency is important to both resonator cavity design engineers and material manufacturers. Having a wide range of custom test cavities, as shown in ***Figure 7***, enables correlated testing to ensure resonator performance in actual applications. ■

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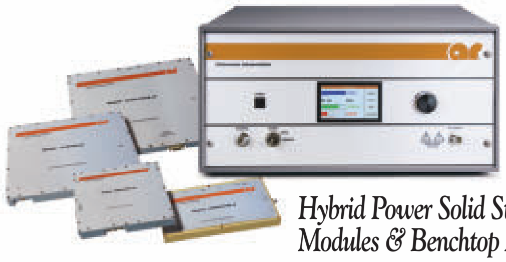

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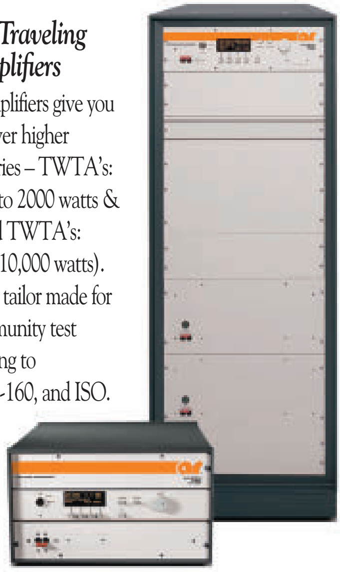

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EM Filter Design Success: The Fast Way

James C. Rautio
Sonnet Software Inc., Syracuse, N.Y.

Port tuning is a powerful technique for achieving first-pass design success. It enables the rapid tuning of complex filter structures with nearly full electromagnetic (EM) analysis accuracy.

After graduating from college in 1978, I designed a set of filters for the Landsat IV GPS preamplifier. Three of the filters were fabricated on alumina substrates. My mentor, Dr. Herbert Thal, one of the world's leading filter designers, had developed some advanced (at the time) filter synthesis and tuning software,[1] allowing the realization of filters that came fairly close to meeting very stringent design requirements – but not quite. In order to obtain design closure, we determined (using our tuning software) how much each resonator length and coupling distance needed to be changed in order to get closer to the required bandwidth, center frequency and group delay dispersion specifications. After re-fabricating each filter and finding we were closer, we repeated the process about three times before we were done.

Later, at Syracuse University, I studied numerical electromagnetics under another world-leading expert, Professor Roger Harrington, the father of the Method of Moments.[2] For the record, Professor Harrington adopted the name "Method of Moments" from some similar work that had already been done in Russia. Many of the techniques that are special cases within the framework of the Method of Moments (e.g., the Galerkin technique and the Rayleigh-Ritz variational technique) had already been developed. It is Harrington's work that provided the over-arching theoretical framework for this branch of numerical electromagnetics and allowed researchers and engineers everywhere to begin using it. This is not unlike Maxwell's work with what we call Maxwell's Equations.

After completing my Ph.D., I started commercializing the numerical EM technique I had developed under Professor Harrington.[3,4] Applying this to filters, instead of repeatedly building filters, we repeatedly analyzed them. EM analysis is much, much faster than building each filter iteration, but it still takes time. Because popular filter designs were becoming more complicated and compact,[5] the old synthesis techniques did not work as well. The number of filter fabrications was significantly reduced through EM analysis, but the required number of EM analyses were getting out of hand.

Dan Swanson developed a technique using Sonnet® where he could EM analyze a filter and include some extra ports on the ends of open-ended stubs used to couple between resonators.[6] For some kinds of filters, this is where capacitive tuning screws are occasionally placed. The tuning screws are used to adjust the resonant frequency of each resonator and tune the filter so that it meets all requirements. Sometimes a bit of luck is required, because coupling between the resonators cannot be tuned this way.

Swanson inserted EM ports in the analysis in place of tuning screws. There was one extra EM port for the open end of each stub. Thus, if there were four open ends, there were six ports in the EM analysis. The extra two ports were for input and output. He would then take the EM analysis results and include them in a circuit theory analysis program such as Keysight's

Advanced Design System (ADS) or NI AWR's Microwave Office® (MWO). In the circuit theory schematic, he terminated the extra EM ports on the open ends of the stubs with an EM analyzed, open-end discontinuity and a short length of circuit theory transmission line. By tuning the short length of transmission line, he could tune the filter to meet its requirements at circuit theory speed, while almost the entire filter had been analyzed, to full EM analysis accuracy. The filter geometry[6] actually has pairs of open ends, so he used EM-analyzed, coupled, open-end pairs and short lengths of coupled transmission line.

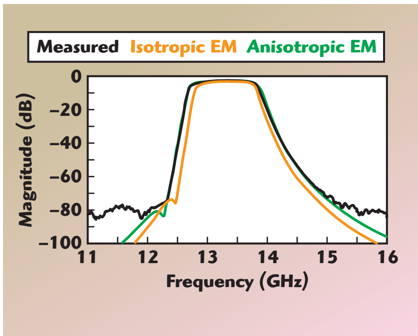
This approach provides circuit theory speed for tuning and optimization and nearly full EM accuracy. The technique still requires some effort by the designer, however, who must determine where to add the tuning ports and draw the schematic that connects the small circuit theory tuning elements. Then it is necessary to determine new dimensions for the filter based on the values of the tuning elements.

Once mastered, its power is significant. For example, when given a filter requirement, one early adopter had a design ready for fabrication the next day. If the specification is similar to a filter already designed, the layout may be ready for fabrication within the hour. Built on multi-layered ceramic, first pass success is assured.

This requires a little more than just the port tuning methodology and EM analysis. For example, ceramics are notorious for being anisotropic, i.e., the dielectric constant depends on direction. An electric field that is perpendicular to the substrate surface experiences one dielectric constant, and an electric field that is parallel to the substrate surface experiences a different one. If EM analysis predicts the correct center frequency, but the wrong bandwidth, it might be due to incorrectly assuming the substrate is isotropic.

FILTER EVALUATION

Figure 1 shows Sonnet's anisotropy capability in the design of a filter, where measured data is compared with the results of Sonnet EM analyses. This illustrates that the calculated bandwidth is different from the actual bandwidth by not including anisotropy, which is corrected when anisotropy is properly accounted for. The isotropic substrate dielectric constant in the simulation is first adjusted to align the EM analysis center frequency with the measurement. Precise measurements of the anisotropic dielectric constants are then used in the Sonnet simulation, which results in the measured and calculated results lying on top of each other. It is important to emphasize that the anisotropic dielectric constants used in the simulation are precisely those that are measured; neither the dielectric constants nor the EM analyzed filter dimensions are altered to achieve these results.



▲ *Fig. 1 The first Sonnet anisotropic EM analysis.*[7]

The fact that nearly all ceramics and ceramic loaded substrate materials are strongly anisotropic may be surprising to some designers. This is because ceramic grains are generally not spherical. During manufacturing, they tend to orient themselves in the same direction as adjacent grains. In some cases, they tend to lie horizontally, especially near the surface. In other cases, they tend to stand vertically. It depends on the manufacturing process. Composite substrates (e.g., epoxy and fiberglass) are also strongly anisotropic. In addition to the anisotropy issue, composite substrates usually have a "butter" layer of epoxy on the top and bottom. For accuracy, these layers should be characterized and modeled as well. Sonnet can analyze anisotropy. Measurement of anisotropy is a matter of building and measuring a few resonators.[7]

Another factor for some substrate materials is metal roughness. Mechanical engineers intentionally increase the roughness on the substrate side of the metal foil in order to improve adhesion. Unfortunately, this also increases loss. The roughness also increases surface inductance, which is not widely known.[8,9] This shifts the

filter passband lower in frequency, an effect that is particularly pronounced in very thin substrates. Inexperienced designers may compensate by incorrectly increasing the substrate dielectric constant. This, correspondingly, increases bandwidth errors in the EM analysis.

Some designers may simply design for a wider or narrower bandwidth and hope that the actual bandwidth of the fabricated filter is on target. This may work for a while, but at some point, the designer will have a need for a new type of filter or a requirement to work over a different frequency range. Then the old rules-of-thumb may no longer suffice.

Sonnet includes models for metal roughness, both increased loss and increased surface inductance, and uniaxial dielectric anisotropy. Including all of these effects is necessary for accurate filter analysis as well as successfully using port tuning for rapid filter design.

Dan Swanson accomplished port tuning by adding EM ports to the ends of the resonators and then adding short lengths of circuit theory transmission line using a circuit theory program. Since his pioneering work, the flexibility and power of the port tuning technique has grown extensively.[10] It has been the subject of considerable research[11,12] and included in filter synthesis software.[13]

MICROSTRIP OPEN-CIRCUIT STUB EVALUATION

Although complex filters can be tuned quickly using this same technique, the approach is best demonstrated with a very simple example, a microstrip open-circuit stub to be tuned to resonance at 25 GHz (see ***Figure 2***). While it may initially seem strange, the first step is to destroy the filter by cutting a very short section out of the stub (see ***Figure 3***). Internal ports are then added on each edge of the gap. These ports are used, through analysis, to "repair the damage" by connecting a short length of circuit theory transmission line across the gap. The initial transmission line length is exactly the same as that removed from the EM analysis.

The quality of these internal ports is critical to the success of port tuning. While the technique can work with nearly any kind of internal port when there is no alternative, errors introduced by uncalibrated or poorly calibrated ports can result in wasteful iterations and incorrect results. Provided the port connecting lines are not overmoded (e.g., they are not radiating), Sonnet's internal ports are calibrated exactly.[14, 15] In addition, these "Co-calibrated™" ports are calibrated in groups with all self and mutual fringing fields between the ports

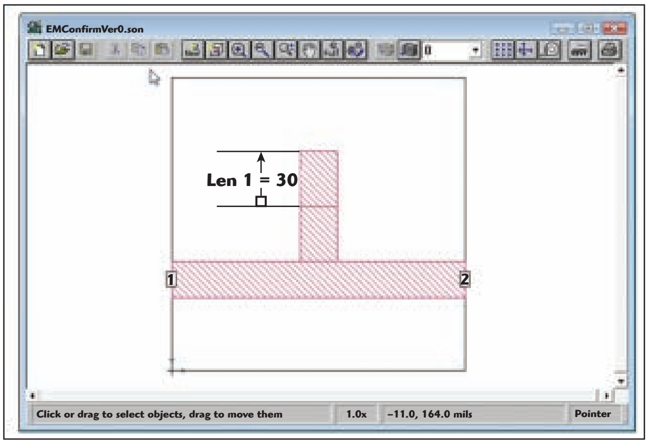


Fig. 2 Microstrip open stub to be tuned to resonance at 25 GHz, demonstrating minimal EM analysis time.

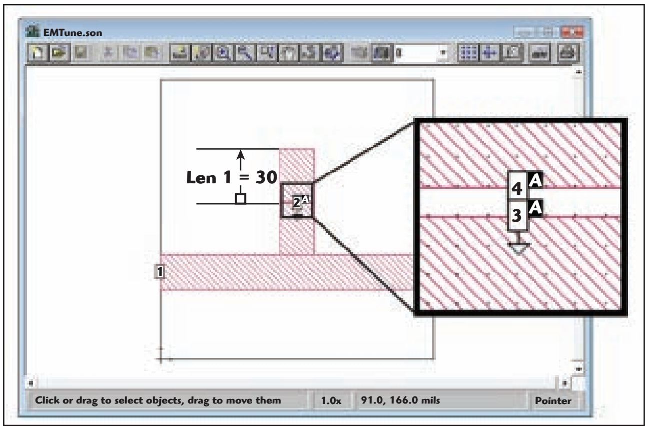


Fig. 3 Open stub filter modified by cutting a narrow gap along the length.

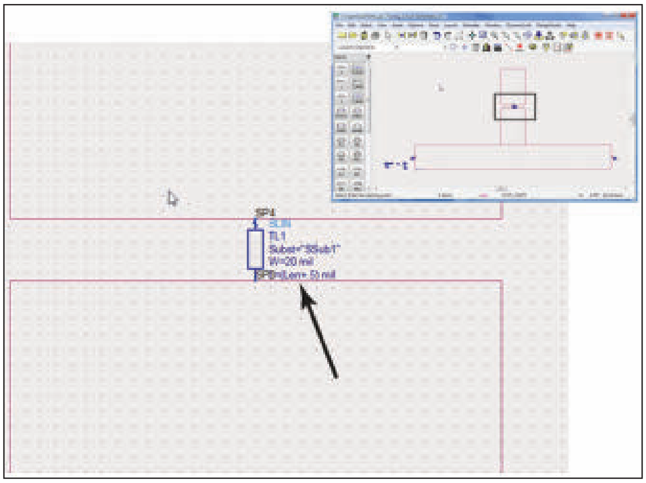
completely removed. A group of ports must all reside on the perimeter of a rectangle. Multiple groups are fine as long as individual groups are separated by more than the port-generated fringing fields.

Accurate and precise calibration is realized because Sonnet analyzes a circuit using an exact Green's function inside a perfectly conducting box.[4,16] The calibration uses the perfectly conducting sidewalls of the containing/shielding box to provide a perfect ground reference for all ports and a perfect short circuit calibration standard. Neither is possible in an unshielded (i.e., no box) approximate Green's function based EM analysis. Thus, when a short section of the stub from the Sonnet EM analysis is removed and replaced with an equivalent length of circuit theory transmission line, the final result is exactly the same – a result which is easily verified. Descriptions of co-calibrated ports are provided by Crupi, et al.,[15] and Rautio.[17] They also provide illustrations of port tuning.

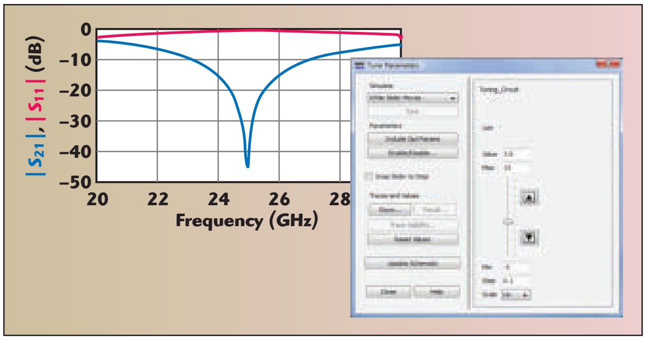
Performing a filter analysis inside a box is important. When used in a system of any kind, most filters must be placed in a conductive box for shielding. The box can strongly influence the in-band filter response,[18] especially at high frequencies where high isolation is often required. For proper design, a filter must be EM analyzed inside the exact box in which it is expected to operate. In contrast, many published filter designs are not contained within a box when built or analyzed, indicating that such filters are never meant for actual application, but are for publication only. An unshielded filter also becomes an excellent antenna at high frequencies. This may be caused by highly over-moded resonators and electrically thick substrates. Rejection looks good when the filter is measured or analyzed in total isolation; however, the unwary designer may be surprised when the filter couples to everything around it.

DESIGN EXAMPLE USING SONNET AND ADS

Sonnet has extensive interoperability with ADS and MWO. Thus, port tuning using Sonnet for the EM analysis and either ADS or MWO for circuit theory tuning is straightforward. For those working on Si RFICs, Sonnet's interface with Cadence Virtuoso allows the same easy design flow. ***Figure 4*** shows the Sonnet result in ADS. In this case, the circuit layout was defined completely inside ADS, sent to Sonnet from ADS by means of an ADS menu selection, and the result automatically loaded back into ADS. Notice that the Sonnet result is shown in the ADS schematic with a convenient layout look-alike schematic symbol, automatically created in Sonnet for use in ADS. Port tuning can result in a large number of ports, so having



▲ *Fig. 4 The open stub filter layout look-alike schematic element generated by Sonnet and automatically loaded back into ADS.*



▲ *Fig. 5 With port tuning, the resonant frequency of the stub is optimized in real time with circuit theory speed.*

a layout look-alike schematic component is exceptionally useful.

A short length of ADS circuit theory transmission line has been inserted between Ports 3 and 4 to "repair the damage" done by cutting the 0.5 mil gap in the stub. The length of the ADS circuit theory transmission line is set with a parameter, Len. The initial resonant frequency of the stub is 27 GHz. By optimizing Len in ADS, the resonant frequency of the stub is tuned to exactly 25 GHz in real time with circuit theory speed (see ***Figure 5***). Len is equal to 3.8 mils, meaning that the length of the stub must increase by 3.8 mils. A confirming EM analysis of the stub with the new length and with the co-calibrated ports removed shows exactly the same result. Len may also be negative if it turns out that a shorter total length is needed for the final design.

The complete circuit is analyzed to nearly full EM accuracy since the circuit theory part of the analysis is very small, the co-calibrated ports are perfectly calibrated (assuming the port connecting lines are not over-moded or radiating) and the EM analysis uses an exact Green's function. The best of both worlds is achieved: tuning at circuit theory speed with nearly full EM accuracy!

CONCLUSION

Port tuning can be used to optimize more than just the length of an open-circuited stub. It can be used to optimize transmission line width and the gaps between transmission lines in more complex filter structures. This technique does require some up-front work by the designer; however, those who avoid it by insisting on having just one button to push will soon wonder why everyone else is producing filter designs so much faster and with more accuracy. The answer is "port tuning."

Full port tuning tutorials using Sonnet with both ADS and MWO are available.[19,20] ■

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Implementation of mmWave AlGaN/GaN HEMTs and Power Amplifier MMICs

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AlGaN/GaN high electron mobility transistors (HEMT) are designed and fabricated based on 0.15 μm gate-length technology. All source electrodes of multi-finger devices are connected to the through-hole ground instead of using air bridges. Device RF measurements show that they can operate at millimeter wave frequencies. Parasitic and intrinsic parameters of the small signal equivalent circuit model are extracted at reverse cut-off and operating bias state. The revised Angelov expressions are adopted to describe nonlinear characteristics, and the large-signal model is constructed using the symbolically defined device (SDD) method. Using these devices, a two-stage, four-channel monolithic microwave integrated circuit (MMIC) power amplifier is realized with 36 dBm output power, 9 dB power gain and 10 percent power-added efficiency (PAE) at 34 GHz.

The AlGaN/GaN HEMT is well suited for use in high frequency power amplifiers due to its high two dimensional electron gas (2DEG) concentration, high mobility and high saturation drift velocity. It can also withstand high operational supply voltages and temperatures.

Because high imaging resolution and system miniaturization are achievable at millimeter wave frequencies, power amplifier research and design using millimeter wave GaN HEMTs and MMICs has attracted a great deal of international interest.[1] Its potential, however, is difficult to realize since GaN technology is complex and immature in the millimeter wave region. Breakdown voltage, output power and power-added efficiency (PAE) are greatly reduced as device physical dimensions become smaller.

This article describes a set of processes for the fabrication of AlGaN/GaN HEMTs and the establishment of equivalent circuit models for a millimeter wave power amplifier. We first design the multi-finger 0.15 μm gate-length GaN HEMTs with an improved source-ground structure and evaluate their frequency characteristics for the millimeter wave application. We then complete parameter extraction of the

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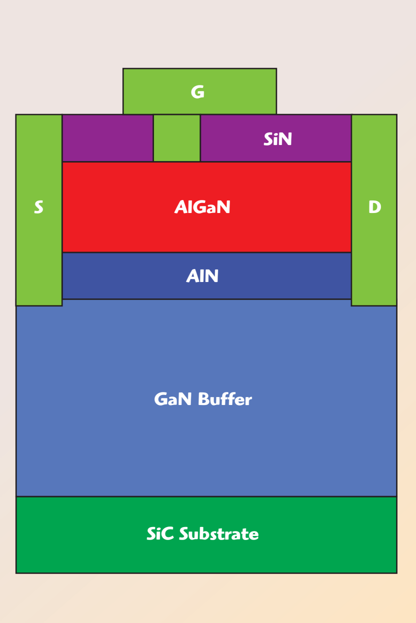
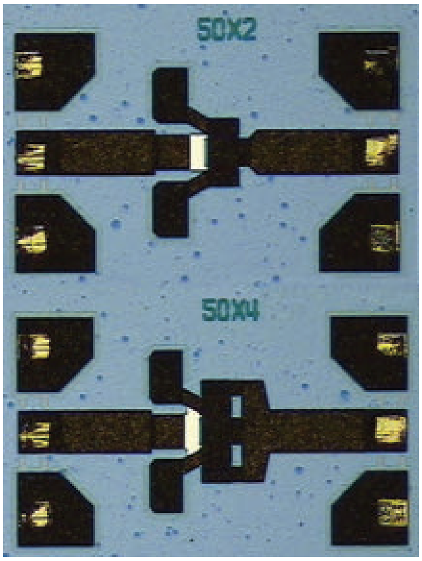
small-signal equivalent circuit model and construct the large-signal model. Finally, we design, fabricate and measure a two-stage four-channel MMIC power amplifier.



▲ *Fig. 1 Single-finger AlGaN/GaN HEMT cross section.*

DEVICE DESIGN AND FABRICATION

A cross-sectional view of a single-finger AlGaN/GaN HEMT structure is shown in ***Figure 1***. The HEMT is grown on a SiC substrate using metal organic chemical vapor deposition (MOCVD). The GaN buffer

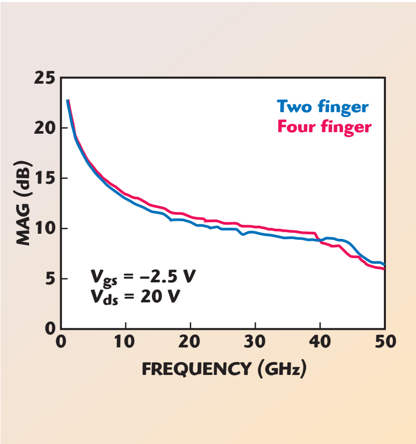


▲ *Fig. 2 Photograph of two and four finger GaN HEMTs.*

layer provides lattice matching with the substrate and exhibits high resistance characteristics. The AlGaN barrier layer is unintentionally doped. The 1 nm thick AlN layer is inserted between the barrier layer and buffer layer to increase the 2DEG in the channel. The SiN passivation layer is added to restrain surface defects in the barrier layer.

The T-gate composed of a Ni/Au alloy is defined using electron-beam lithography. The gate length is 0.15 μm and the gate-cap length is 0.5 μm. The gate-drain cap is longer than the gate-source cap in order to decrease the electric field in the barrier layer and channel. A Ti/Al/Ni/Au alloy is evaporated to form source and drain electrodes through rapid thermal annealing. The ohmic contact resistance is 0.3 ohm-mm. The source-drain distance is optimized to be 3.5 μm.[2] Through-hole ground technology is used with all the source electrodes connected to the holes. This new structure solves the source ground problems of multi-finger HEMTs that employ air bridges, reducing source parasitic inductances. Photographs of two finger and four finger devices with 50 μm single-finger gate-widths are shown in ***Figure 2***.

S-parameters of the two HEMTs are measured from 0.1 to 50 GHz at V_{gs} = -2.5 V and V_{ds} = 20 V respectively. Assuming input and output matching, maximum available gain (MAG) is calculated using the S-parameters and is shown in ***Figure 3***. It is apparent that there is little difference between the two finger and four finger devices, indicating that the multi-finger HEMT does not increase source inductance. The MAG of the two finger



▲ *Fig. 3 Small-signal gains at V_{gs} = –2.5 V and V_{ds} = 20 V.*

HEMT can reach 9.6 dB at 30 GHz while that of the four finger HEMT can reach 10.2 dB. This rise may be due to paralleling of the parasitic resistances.

EQUIVALENT CIRCUIT MODEL

To design an amplifier, the device equivalent circuit model must be derived. This requires de-embedding of coplanar waveguide (CPW) test pads and lead wires. The thru-reflect-line (TRL) method is used, employing the three calibration structures shown in ***Figure 4***.[3] The S-parameters of the core device are determined after de-embedding.

The small-signal equivalent circuit model is shown in ***Figure 5***. L_g, L_d and L_s are parasitic lead inductances of the GaN HEMTs. R_g, R_d and R_s are parasitic resistances. C_{gs}, C_{gd}, C_{ds}, R_i, R_{ds}, G_m and t are intrinsic parameters which are related to the gate and drain voltages. All of these parameters can be determined for different bias voltages. The reverse cut-off method is used to extract the parasitic inductances and resistances. Parasitic parameters are ignored when the frequency is lower than 5 GHz at V_{gs} = -6 V and V_{ds} = 0 V. Under this condition only C_{gs}, C_{gd} and C_{ds} exist in the intrinsic region and they are easily obtained. Then the frequency is increased to 50 GHz to obtain the parasitic inductances and resistances. The intrinsic parameters are determined at V_{gs} = -2.5 V and V_{ds} = 20 V based on Y-parameters, after removing all the parasitic parameters.

Nonlinear characteristics are determined by fitting nonlinear expressions at different gate and drain voltages. The Angelov empirical formulas can be used to describe the I-V and C-V large signal property of GaN HEMTs:[4]

$$I_{ds} = I_{max} * (1+\tanh(a)) * \tanh(b * V_{ds}) * \exp(c * V_{ds}) \quad (1)$$

$$a = P1 * (V_{gs} - V_{max}) + P2 * (V_{gs} - V_{max})^2 + P3 * (V_{gs} - V_{max})^3 + \cdots \quad (2)$$

$$C_{gs} = C_{gs}0 * (1+\tanh(a1)) * (1+\tanh(a2)) \quad (3)$$

$$C_{gd} = C_{gd}0 * (1+\tanh(a3)) * (1-\tanh(a4)) \quad (4)$$

$$a1 = d0 + d1 * V_{gs} + d2 * V_{gs}^2 + d3 * V_{gs}^3 + \cdots \quad (5)$$

$$a2 = e0 + e1 * V_{ds} + e2 * V_{ds}^2 + e3 * V_{ds}^3 + \cdots \quad (6)$$

$$a3 = f0 + f1 * V_{gs} + f2 * V_{gs}^2 + f3 * V_{gs}^3 + \cdots \quad (7)$$

$$a4 = g0 + (g1 + g * V_{gs}) * V_{ds} + g2 * V_{ds}^2 + g3 * V_{ds}^3 + \cdots \quad (8)$$

I_{max} and V_{max} are the source-drain current and gate voltage when the transconductance reaches the maximum. $C_{gs}0$ and $C_{gd}0$ are the gate-source and gate-drain capacitances at zero bias. The other parameters in the formulas are fitting coefficients. For the high order polynomials, the needed precision can be satisfied by evaluating them to the third order. The I-V formula should be modified, however, to reflect self-heating under diverse gate voltages. It is revised as follows:

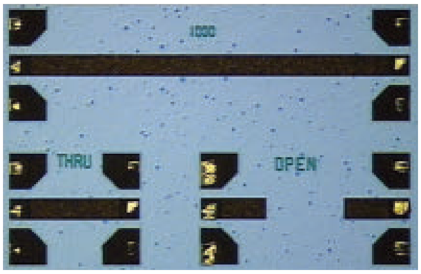
$$I_{ds} = I_{max} * (1+\tanh(a)) * \tanh(b * V_{ds}) * (1 + c * \tanh(V_{gs}) * V_{ds}) \quad (9)$$

Here, it is mainly considered that the gate voltage should be added to the section that describes saturation characteristics for this change. Other intrinsic parameters have little impact at different gate voltages, so average values may be used.

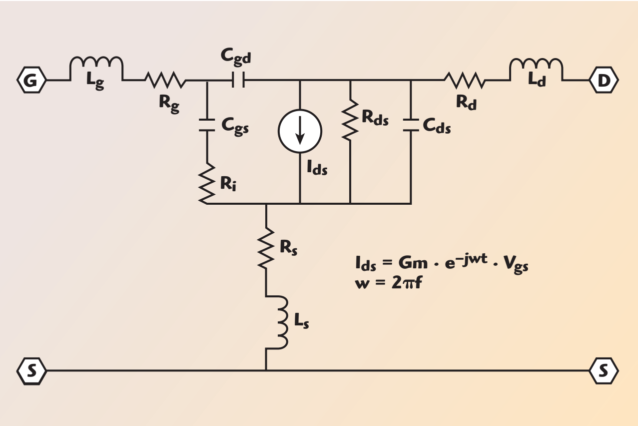
The large-signal equivalent circuit model with nonlinear fitting expressions can be implemented by using the SDD form during the circuit design process (see ***Figure 6***). Based on the port voltages and currents, this method can reflect large signal characteristics as the intrinsic parameters change along with the bias voltages. The model parameters of multi-finger and different gate-width GaN HEMTs can be obtained through parallel and linear relationships.[5]

POWER AMPLIFIER MMIC REALIZATION AND MEASUREMENT

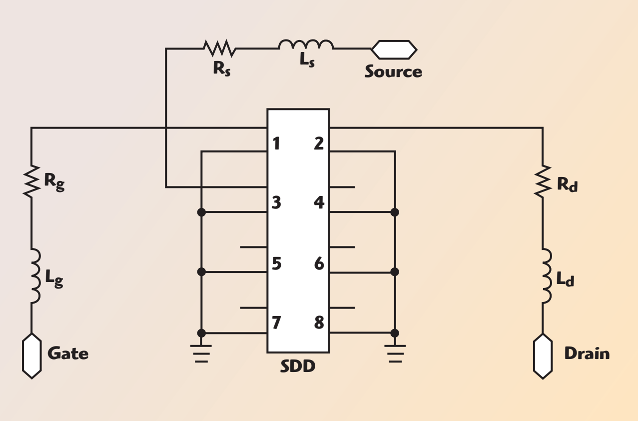
The MMIC power amplifier is designed and fabricated using the multi-finger GaN HEMT equivalent circuit models. In addition to the active devices, some passive components such as microstrip lines, capacitances, resistances and through-holes are needed. The equivalent circuit



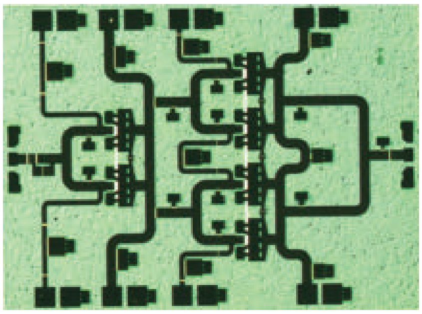
▲ *Fig. 4 TRL calibration structures.*



▲ *Fig. 5 Small-signal equivalent circuit model.*



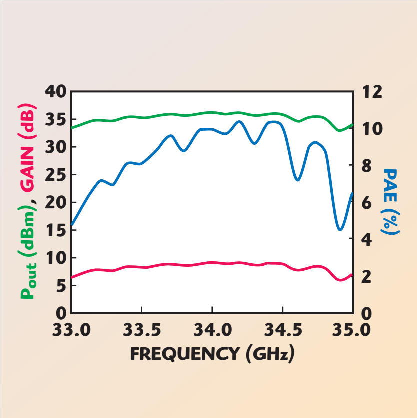
▲ *Fig. 6 SDD large-signal equivalent circuit model.*



▲ *Fig. 7 MMIC power amplifier.*

models of these passive devices are obtained through 3-D electromagnetic simulation.

The MMIC is designed with a two-stage, four-channel topology.[6] The front end combines two 8 × 60 μm GaN HEMTs. The output stage consists of four 8 × 75 μm GaN HEMTs. The matching circuits of each stage are optimized based on the source and load-pull method. The input and output ports are CPW, and the port impedances are matched to 50 ohms. Stability measures are incorporated to prevent self-oscillation. The fabricated circuit is shown in ***Figure 7***. Its total area is 3.3 × 2.5 mm.



▲ *Fig. 8 MMIC power amplifier measured performance.*

The MMIC is measured on wafer. The 24 V drain bias supply is pulsed with a 10 μs pulse width and 10 percent duty cycle, and the gate bias is set to 2.5 V for both stages. With an input power of 27 dBm under CW operating conditions, the measured performance is shown in ***Figure 8***. The output power is higher than 33 dBm over the entire 33 to 35 GHz band, and the maximum output power is 36 dBm at 34 GHz with 9 dB gain and 10 percent PAE.

CONCLUSION

Multi-finger 0.15 μm gate-length AlGaN/GaN HEMTs designed with improved source electrode structures effectively solve the grounding problems of multi-finger HEMTs employing air bridges. A GaN MMIC power amplifier designed using these devices yields 36 dBm output power, 9 dB power gain and 10 percent PAE at 34 GHz. ■

ACKNOWLEDGMENT

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INVITED PAPER

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Improving the Second Harmonic Rejection of Side-Coupled Filters

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Galormic, Qiryat Tivon, Israel
Benny Haddad, Jaakko Juntunen
National Instruments, Austin, Texas

Filters are used in communications systems to keep unwanted signals from propagating through a network. These signals may be interferers from other systems, or they may be generated by the nonlinear behavior of components within the network.

Side-coupled filters constructed from microstrip on printed circuit boards (PCB) are widely used throughout the industry because of their low cost and manufacturability. A side-coupled filter, also known as a parallel edge-coupled filter,[1] is built by combining several sections of coupled transmission lines, in which each section is offset from the previous section. In addition to a relatively large footprint, one of the drawbacks of the side-coupled filter is limited rejection of the second harmonic. This application note demonstrates a design approach that reduces this problem: adding notch filters improves the rejection without significantly affecting the filter's passband performance.

From user-defined filter characteristics, such as the passband frequencies, passband ripple and rejection at the stopband, an initial filter design was created using the filter synthesis tool in NI AWR Design Environment™ Microwave Office. The resulting circuit (see ***Figure 1a***) defines the microstrip layout for manufacturing and electromagnetic (EM) analysis. The filter's simulated performance is shown in ***Figure 1b***.

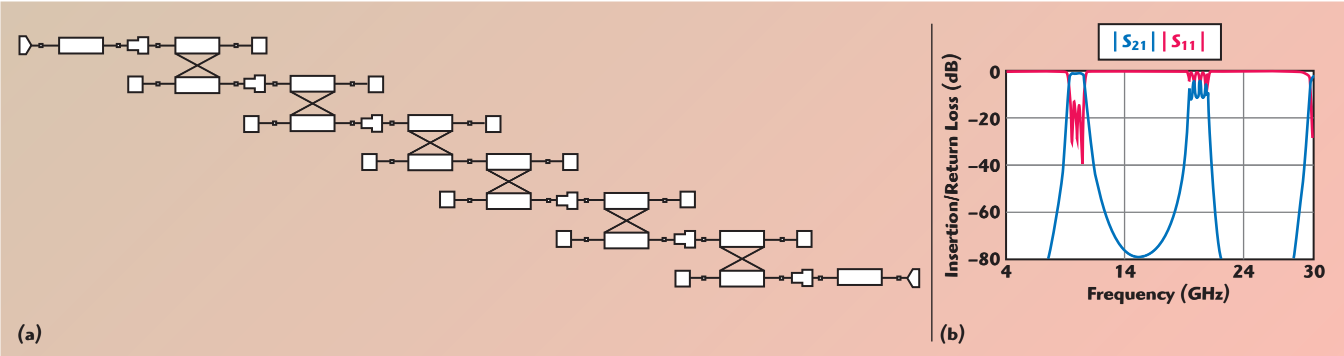

Fig. 1 The schematic topology of the initial filter design (a) and modeled $|S_{21}|$ and $|S_{11}|$ responses (b).


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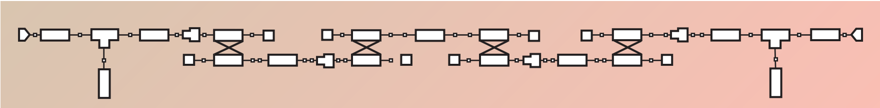

Fig. 2 *The schematic topology of a tapped in-line side-coupled filter.*

To reduce susceptibility to EM interference, the filter can be housed in a closed channel or waveguide. There is a risk, however, of higher-order waveguide modes unless the waveguide's cutoff frequency is higher than the highest rejection frequency. In this design example, transmission lines are added between the pairs of coupled lines, allowing the pairs to be rearranged so they are in-line.[2] This change results in a narrower footprint, enabling a waveguide with a higher cutoff frequency to be used to house the filter. ***Figure 2*** shows a topology of a tapped in-line side-coupled filter[3] with the added microstrip lines between all pairs.

ADDING NOTCH ELEMENTS

To improve second harmonic rejection, open circuit microstrip stubs are added to the filter. They are sized to be a quarter wavelength long at the second harmonic of the passband center frequency. At the second harmonic, the stub's open circuit impedance will be transformed to a short circuit on the transmission line that connects the coupled pairs. This short suppresses the second harmonic of the passband. The capacitive loading of the open stub in the passband will only slightly impact the performance.

Figure 3a shows how the open stub is inserted in the side-coupled filter, by adding interconnecting transmission lines between the coupled-line pairs. The design can be made more compact, especially for higher frequencies, by flipping the stub upwards (see ***Figure 3b***). The stubs make the filter wider, even if flipped; using radial stubs and bending them will help minimize the footprint. Optimizing the circuit model, then analyzing the EM performance, led to the layout shown in ***Figure 4***.

The filter dimensions enable it to be housed in a WR22 waveguide, which has a cutoff frequency of 26.3 GHz. The simulated insertion loss and return loss of the filter are plotted in ***Figure 5***, comparing the performance

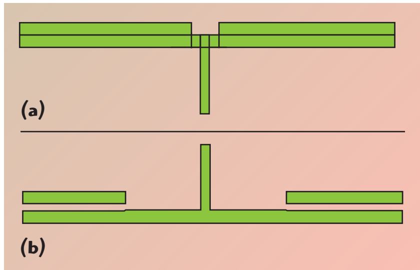

Fig. 3 *A second harmonic notch filter inserted between the coupling sections (a) and with the notch filter flipped upward to reduce the area of the filter (b).*

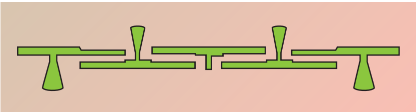

Fig. 4 *Radial stubs are used to reduce the size of the bandpass filter with notch filtering.*

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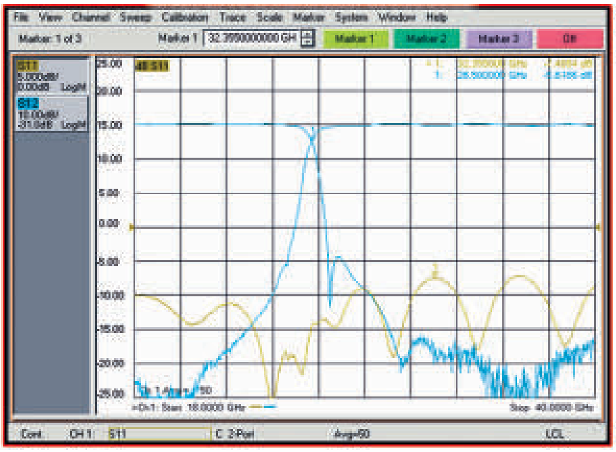

• INSERTION LOSS	2.0dB
• VSWR	2.5:1
• K BAND PASSBAND	18GHz Min., 25GHz Max
• Ka BAND PASSBAND	28GHz Min., 40GHz Max
• K BAND REJECTION	32 to 46GHz, >60dBc
• Ka BAND REJECTION	DC to 22GHz, >60dBc
• SIZE	0.80" X 0.60" X 0.38"

20 to 40GHz High Pass Filter

• INSERTION LOSS	1.5dB
• VSWR in PASSBAND	2.0:1
• 1dB CUTOFF	20GHz
• REJECTION	DC to 14.5GHz, >54dBc
• SIZE	0.614" X 0.50" X 0.56"

18 to 26.5GHz High Pass Filter

• INSERTION LOSS	1.5dB
• PASSBAND	18 to 26.5GHz
• VSWR in PASSBAND	2.0:1
• REJECTION	DC to 15GHz, >60dBc
• SIZE	0.64" X 0.58" X 0.38"

26.5 to 40GHz High Pass Filter

• INSERTION LOSS	2.0dB
• VSWR in PASSBAND	2.0:1
• 1dB CUTOFF	26.5GHz
• REJECTION	DC to 20GHz, >54dBc
• SIZE	0.65" X 0.65" X 0.50"

DC to 26.5GHz Low Pass Filter

• INSERTION LOSS	1.5dB
• PASSBAND	DC to 26.5GHz
• VSWR in PASSBAND	2.2:1
• RIPPLE	+/-0.75dB Max
• REJECTION	28.5 to 40GHz, >25dBc
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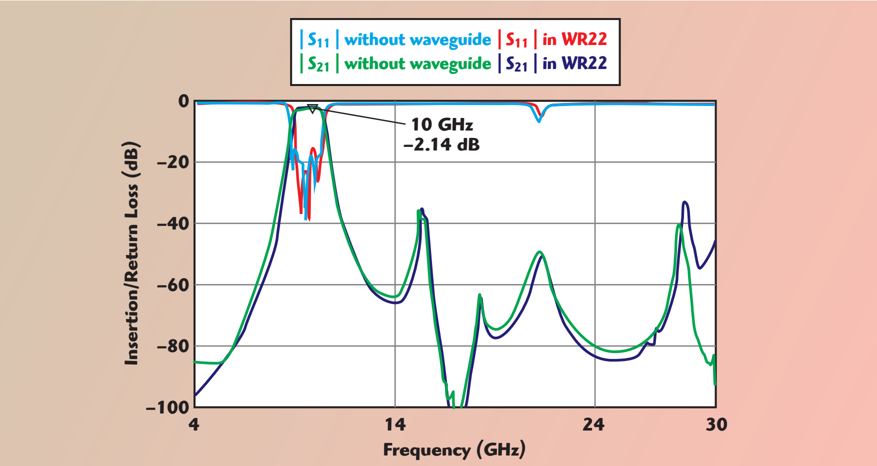


▲ *Fig. 5 Simulated responses of the open microstrip filter (blue and green) and inside a WR22 waveguide (red and purple).*

in waveguide to open microstrip. While there is a slight upward frequency shift of the filter in waveguide, the second harmonic rejection is as good as before. Since the waveguide changes the filter response, a fine-tune redesign is necessary.

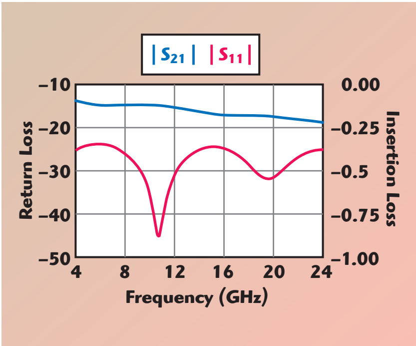
The coax to connector model can be included in the design using the Analyst™ 3D finite element method (FEM) EM simulator. Separately, the coax-to-microstrip transition can also be modeled and, if necessary, a matching section can be added. Looking at the connector transition alone (see ***Figure 6***), there is no significant mismatch up to the second harmonic, and the insertion loss of 2 × 0.11 dB = 0.22 dB in the passband is as expected.

The geometry and mesh shown in ***Figure 7*** was used for the complete simulation, resulting in the filter response shown in ***Figure 8***. Insertion loss has increased 0.15 dB, and the second harmonic rejection is better than 50 dB. The WR22 waveguide and connectors protect the filter from any outside interference without significantly changing the filter response.

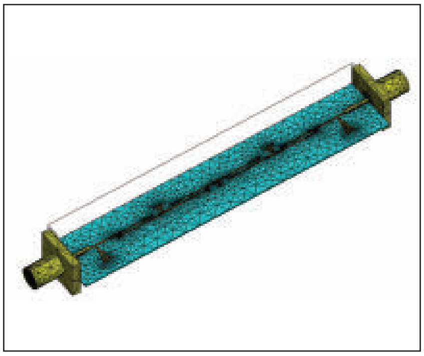
For comparison, the same filter was simulated in a WR42 waveguide, which has a 14.1 GHz cutoff; the results are also shown in Figure 8. The second harmonic rejection is 30 dB less, since WR42 is big enough to propagate at the second harmonic, leading to considerably poorer rejection.

CONCLUSION

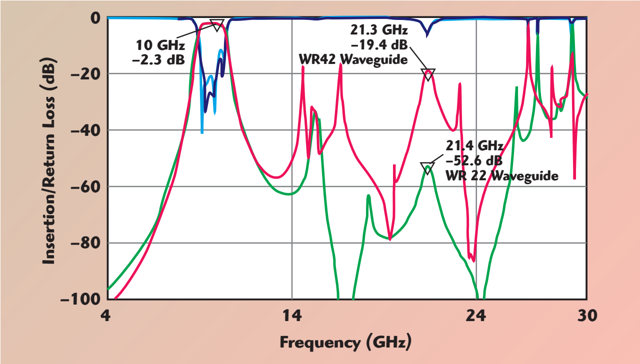
The use of an in-line topology for a side-coupled microstrip filter results in a narrower footprint with minimal impact on filter performance. Incorporating notch filters for second harmonic rejection is practical and achieves 50 to 60 dB rejection with minimal degradation in the passband performance. For a filter mounted in waveguide or a closed channel, the side-coupled topology improves the rejection of higher frequencies up to the waveguide cutoff. ■



▲ *Fig. 6 Return loss and insertion loss of the coax-to-microstrip transition.*



▲ *Fig. 7 Composite model of the filter in the WR22 waveguide, including the coax connectors.*



▲ *Fig. 8 Simulated responses of the filter integrated in WR22 (solid line) and WR42 (dashed line) waveguides, including the coax connectors.*

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INVITED PAPER

High Dynamic Range IF Receiver Simplifies Point-to-Point Design

Paul Hendriks
Analog Devices, Norwood, Mass.

Microwave point-to-point links are an integral part of a cellular mobile network. Known as backhaul, they link cell sites (the BTS or Node B) and the radio controllers (the BSC or RNC) in over 50 percent of the global deployments, where fiber links are not cost effective. The market's shift to smartphones has increased data traffic (e.g., streaming video), which is driving the capacity of microwave backhaul.

To scale the data throughput of the point-to-point radio network to meet the needs of LTE and LTE-Advanced, future generations of microwave links will need to:

- Move to higher-order digital modulation, from today's 256 QAM to as high as 4096 QAM. This will provide a 50 percent increase in capacity for a fixed channel bandwidth.
- Support channel bandwidths from 56 to 112 MHz in the traditional 6 to 42 GHz bands. Every doubling of channel bandwidth provides a proportional increase in the data throughput rate if the carrier-to-noise ratio (CNR) remains constant.
- Employ techniques such as polarization diversity, channel aggregation and n × n line-of-sight multiple-input-multiple-output (MIMO).

As is typically the case in communication system design, this increase in throughput capability comes at a price. Receiver sensitivity drops by 3 dB for every doubling in QAM or bandwidth, while the dynamic range of the link must increase to improve the error vector magnitude (EVM) performance.

Traditional backhaul systems split the radio into indoor (IDU) and outdoor (ODU) units. The RF/microwave section is in the ODU and connected with a coaxial cable to the rest of the system in the IDU. The cable, which can be up to 300 meters long, carries bidirectional traffic; a diplexer separates the receive (Rx) IF signal, centered at 140 MHz, from the transmit (Tx) IF, which is centered between 340 and 400 MHz.

The industry is moving to a single, self-contained outdoor unit (ODU), where the radio modem and transceiver are combined with the switching/multiplexing and traffic interface in a


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single box that is mounted on a tower or other structure. This trend is motivated by minimizing capital and operating expenses (CAPEX and OPEX) at new sites and limited space at existing sites. However, the legacy split IDU/ODU configuration will remain the majority of point-to-point shipments for the foreseeable future.

MODEM TRANSCEIVER DESIGNS

Given this evolving market, the back-end modem transceiver architecture should increase capacity and be compatible with both the legacy IDU/ODU and next generation ODU platforms. Additional design goals are to simplify the block diagram, relax the filtering and AGC requirements and reduce cost.

Recent advances in high speed digital-to-analog converters (DAC) and analog-to-digital converters (ADC) – operating at clock rates well above 1.5 GSPS – enable synthesizing and digitizing QAM signals at high IF frequencies with exceptional accuracy. DACs and ADCs now support 4096 QAM and eliminate the quadrature error correction that is usually required for analog IQ implementations. Their high dynamic range and oversampling ratio allow the majority of the filtering to be performed digitally, which reduces analog filtering and the digital equalization to compensate for it.

In the Tx path, high speed DACs are replacing the traditional dual DAC and IQ modulator implementations. They can synthesize the wideband QAM signals with exceptional EVM performance and do not require Tx calibration.

In the Rx path, most of the functionality of the IF receiver can be integrated into a single IC. The AD6676 is one such wideband IF subsystem; a block diagram of the IC is shown in ***Figure 1***. Based on a bandpass sigma-delta (ΣΔ) ADC, it handles IF signal bandwidths up to 160 MHz, operating with an internal clock rate of up to 3.2 GHz. The high oversampling capability of the ΣΔ ADC greatly simplifies IF analog filtering requirements. ADCs operating at lower sampling rates require filtering to suppress adjacent channels and interference/blockers that would otherwise "alias" back onto the IF signal and reduce the receiver's sensitivity.

The ADC in the AD6676 has a high dynamic range, with a noise spectral density (NSD) floor of -160 dBFS/Hz for narrowband QAM channels. This improves the analog AGC range, to compensate for fading, and reduces the required diplexer Tx-to-Rx isolation. The Rx subsystem includes a 27 dB digital attenuator with 1 dB resolution that can be used to calibrate the static gain error, caused by initial component tolerances and the variation in coaxial cable loss.

The high speed DAC in the Rx IF subsystem both enhances performance and simplifies the IDU transceiver. ***Figure 2a*** shows the block diagram of a direct conversion transceiver with Rx and Tx IFs of 140 and 400 MHz, respectively. The challenges of direct conversion transceiver archi-

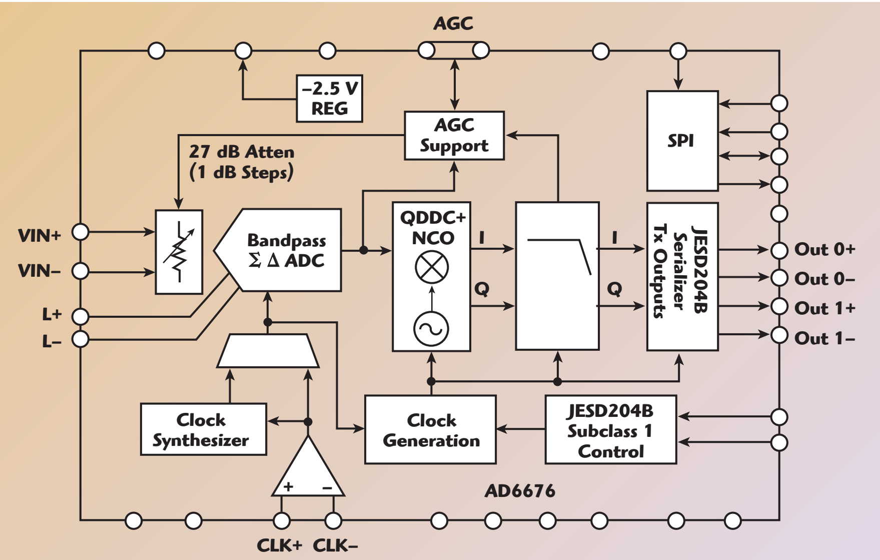
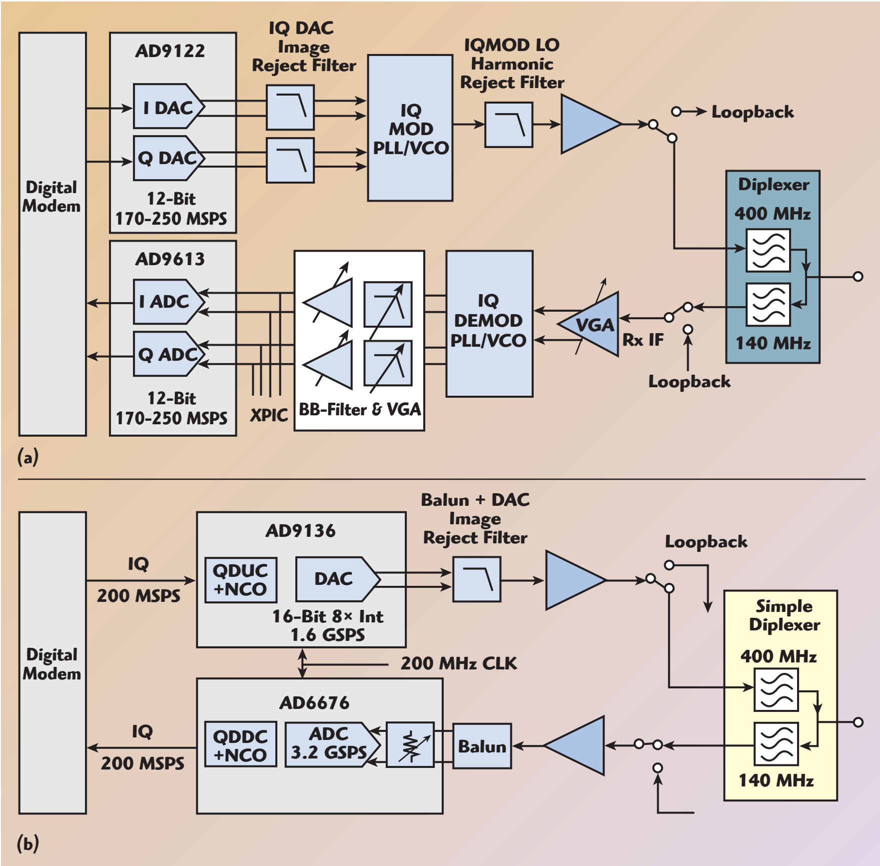


Fig. 1 Block diagram of the AD6676 wideband IF receiver subsystem.

tectures are well documented. They can be overcome with IQ balance calibration, DC offset correction, tunable baseband IQ filtering and careful design of the diplexer to suppress Tx leakage. While transceivers with 256 QAM and channel bandwidths of 56 MHz are in production today, increasing the QAM constellation by 8× or more and doubling the channel bandwidth pose significant challenges to the direct conversion architecture. However the recent advances in high speed ADC and DAC technology enable a digital IDU architecture, as illustrated in ***Figure 2b***. This transceiver requires only four ICs and delivers nearly perfect performance, with significantly relaxed filtering requirements.

A high speed DAC operating at a clock rate of 1.6 GSPS can synthesize a 112 MHz, 1024 QAM Tx signal with exceptional EVM performance. This allows the majority of the Tx link error budget to be reserved for the ODU, where the additive effects of phase noise and linearity degrade EVM the most. While a lowpass filter is required to suppress the first DAC image at 1.2 GHz, it can be relaxed up to 12 dB relative to the LO harmonic reject filter, which is needed to filter the IQ modulator's third-order LO image that also falls at 1.2 GHz. Transmit power control to overcome cable losses can be performed within the IC, with negligible degradation of the EVM over a 15 dB range.

On the Rx side, the AD6676 digitizes the 112 MHz, 1024 QAM channel with excellent dynamic range and accuracy (see ***Figure 3***), even with a large amount of Tx leakage from the "relaxed" diplexer filter. In this figure, the receiver subsystem was configured to support 112 MHz of channel bandwidth with its attenuator set to 3 dB, such that the effective noise figure referred to the input of the preamplifier was around 10 dB. The fast Fourier transform (FFT) response of the ΣΔ ADC data output (used only for the demonstration) is shown in ***Figure 3a***. A CW tone of -17.2 dBm at 143 MHz represents the signal; the Tx leakage is centered at 400 MHz, with a power of -26 dBm.



▲ *Fig. 2 Comparison between legacy direct conversion IDU transceiver architecture (a) and architecture using high speed DAC and ADC for direct digital synthesis and digitization of the Tx and Rx QAM signals (b).*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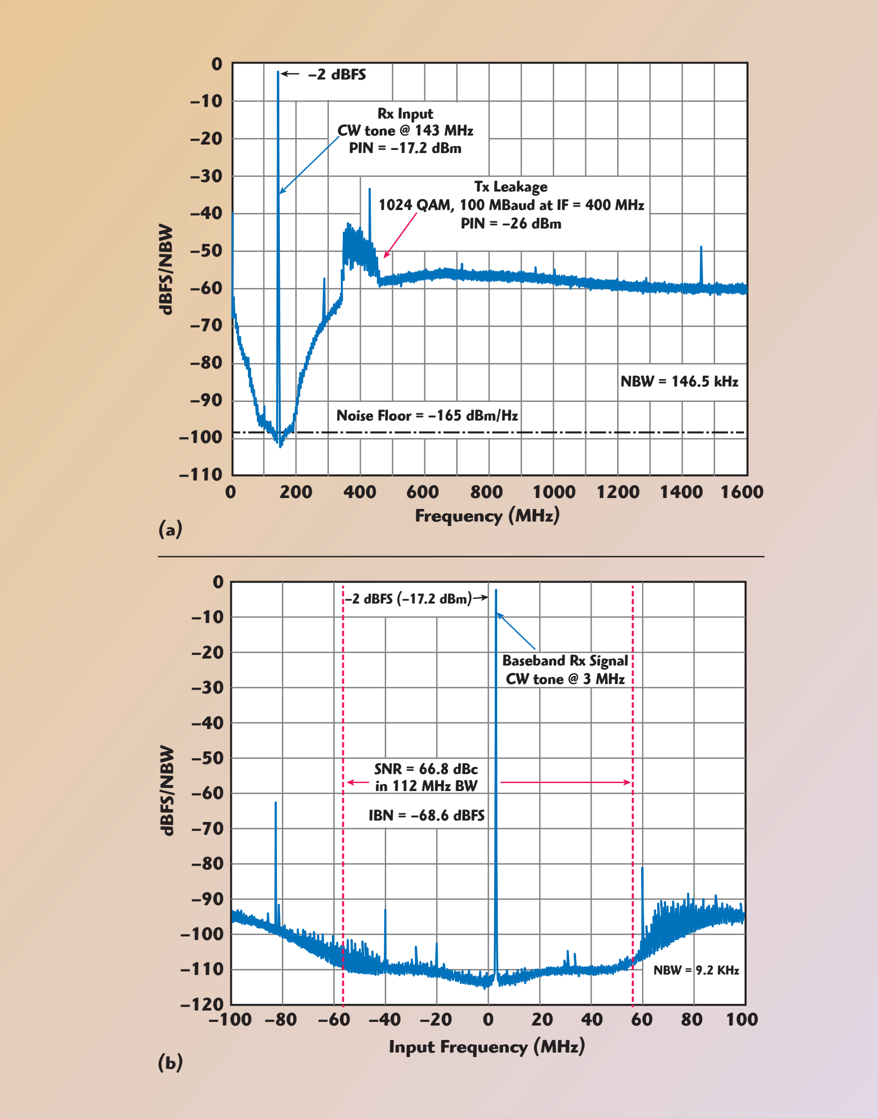
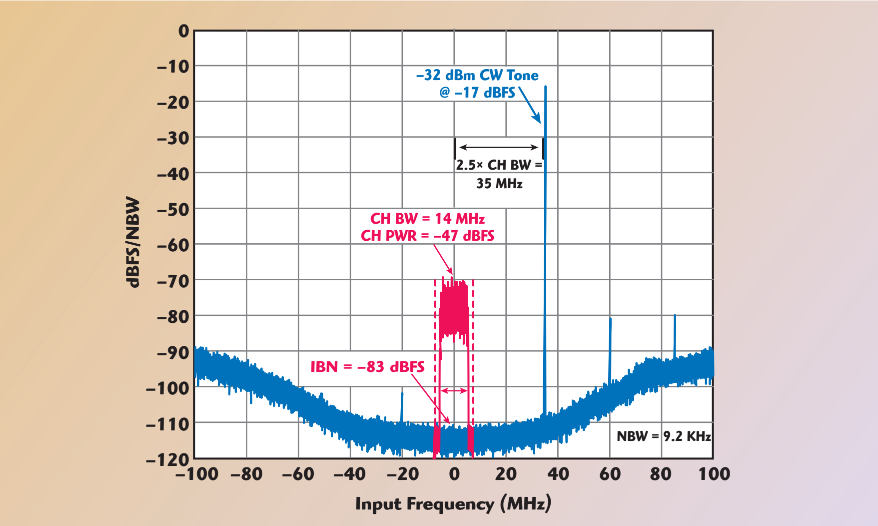
ApplicationNote



▲ *Fig. 3 FFT of the AD6676 ADC output showing the spectrum of a CW signal with Tx leakage (a) and FFT of the IQ data following digital down-conversion (b).*



▲ *Fig. 4 FFT of the IQ data showing the high dynamic range of the ADC provides design margin to tolerate adjacent interferers.*

The inherent "noise shaping" of the tunable bandpass ΣΔ ADC is evident in the region of high dynamic range centered about the desired IF, where the noise floor drops to -160 dBFS/Hz. ***Figure 3b*** plots the "zero IF" FFT response of the 16-bit, 200 MSPS IQ data after digital down-conversion and 16 × decimation filtering. The digital filter provides 85 dB rejection to remove the out-of-band noise and Tx leakage signal from aliasing back into the 112 MHz passband. The residual shaped noise falling outside the 112 MHz passband is removed by the modem's root-raised-cosine (RRC) filters.

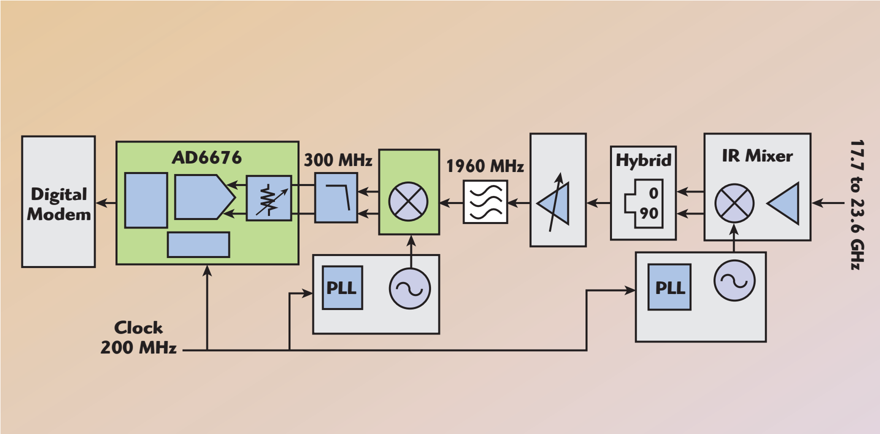
With this large CW signal of -2 dBFS, the in-band noise (IBN) was -68.6 dBFS. If a full-scale 1024 QAM Rx signal with a 10 dB peak-to-rms were to replace this CW tone, 7 dB of additional back-off would be required to prevent the ADC from clipping. In this case, the Rx IDU input power would be at -9 dBFS (-24.2 dBm), suggesting a CNR of nearly 60 dB.

To simplify the diplexer filter design, the diplexer Tx-to-Rx rejection would now be roughly 20 dB to suppress a -6 dBm Tx signal, such that the Tx leakage power would be -26 dBm at the input of the Rx preamp. For deployments with shorter cable runs between the IDU and ODU, the attenuator would be increased to tolerate higher QAM levels from the ODU.

The ability of the IDU receiver to recover a QAM signal at very low sensitivity levels in the presence of an unwanted signal nearby is an important specification (BER $\leq 10^{-6}$ with forward fault correction enabled). Perhaps the most demanding test (per ETSI EN 301 390 V1.2.1) is when a CW interferer tone (blocker) with 30 dB higher power than the QAM signal is only a 2.5× channel offset from the desired signal. Tunable or switched-bank filters employed in today's receivers are mostly driven by this specification, since the modem must support channel bandwidths from 3.5 to 56 MHz. The previous example represents the next generation 112 MHz channel bandwidth case, where it is assumed that the adjacent CW interferer is sufficiently suppressed by a 112 MHz fixed channel filter that also performs image rejection, prior to the last down-conversion within the RF chain of the ODU. This same filter should provide sufficient blocker rejection at offsets of 70 and 140 MHz for the 28 and 56 MHz channel bandwidth cases. However, for channel bandwidths of 14 MHz or less, the CW tone will fall within this filter's passband; this signal needs to be rejected with additional bandpass filtering at 140 MHz or digitized by the ADC and digitally filtered.

ADVANCED ARCHITECTURES

An advanced ADC IDU receiver architecture has the instantaneous dynamic range to support this scenario without extra filtering. ***Figure 4*** shows the FFT frequency response of the same Rx line-up used in Figure 3 except that the ΣΔ ADC's tunable bandwidth was reduced to 56 MHz. In this example, a -32 dBm CW tone at 175 MHz (or 35 MHz offset) was



▲ *Fig. 5 Block diagram of dual down-conversion ODU radio using the wideband IF receiver subsystem.*

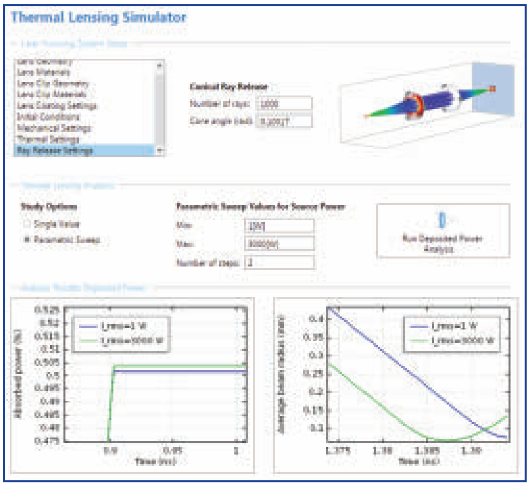
added to the ever present -26 dBm Tx leakage signal at 400 MHz. This CW tone corresponds to a -17 dBFS input level seen by the ADC and is set to be 30 dB higher than a -47 dBFS 1024 QAM signal at minimum sensitivity (CNR = 36 dB). The CW interferer can be increased by an additional 15 dB, highlighting the design margin that can be allocated to the microwave circuitry's noise contribution. In the absence of the blocker, the desired 1024 QAM signal level can be increased by 38 dB, offering additional dynamic range for the IDU receiver to compensate for fading.

The same dynamic range benefits that an advanced ADC offers for the IDU design can be used in a self-contained ODU receiver design. ***Figure 5*** shows the receiver block diagram for an 18 to 23 GHz ODU with dual down-conversion prior to the IF receiver. Other microwave bands in the 6 to 43 GHz range can be supported with the same IF receiver subsystem by selecting the appropriate image reject mixers, phase-locked loops and, possibly, changing the first IF frequency.

With a single ODU, where there is no cable to limit the IF choices, the ADC can be set to a higher IF, such as 300 MHz, which further simplifies the RF image-rejection filtering. The ADC can connect directly to the RF mixer or, should any of the larger mixer spurs require additional suppression, via a simple third-order lowpass roofing filter. The RF filter at 1960 MHz handles channel bandwidths up to 112 MHz. With the ADC attenuator at 0 dB, the combined noise floor is below -157 dBFS/Hz for channel bandwidths of 56 MHz, which is an equivalent NF of 17 dB. The default total conversion gain can be initially optimized with the instantaneous dynamic range, such that the digital modem tracks initial fading from nominal Rx input power levels. The AGC threshold can be set to increase the gain when the modem's Rx BER drops below a predetermined level for a specified QAM signal level. This hybrid approach only activates the RF AGC if the input levels are very low, to improve the receiver's minimum sensitivity level.

CONCLUSION

To increase data rates, next generation microwave point-to-point radios will utilize higher QAM modulation and channel bandwidths up to 112 MHz, and they must have the dynamic range to maintain BER performance with signal fading. Advances in ADC and DAC technology are enabling modem transceivers to support these changes, while also simplifying the architecture. For split IDU/ODU systems, wideband IF receivers such as the AD6676 offer exceptionally high dynamic range to ensure excellent modulation accuracy (EVM) in the presence of adjacent interfering signals, without needing complicated tunable or bulky switched-bank filters. For single ODU systems where the receiver can directly interface with the down-converting mixer, the high instantaneous dynamic range of the receiver reduces RF filtering requirements and the RF AGC range to compensate for fading. ■



COMSOL Multiphysics® 5.0 Introduces the Application Builder

COMSOL
Burlington, Mass.

COMSOL recently released COMSOL Multiphysics® 5.0 with extensive product updates, three new add-on products and the new and revolutionary Application Builder.

Current computational tools are often so complicated to use that very few engineers are trained to do it – at least compared to the number of potential beneficiaries. Developed to meet this growing need for more accessible simulation, the Application Builder allows research and development engineers to package their COMSOL models into easy-to-use applications that can be run by anyone. Simulation apps can then be distributed using COMSOL Server™, allowing design teams, production departments and others to use the applications with a Windows client or web browser.

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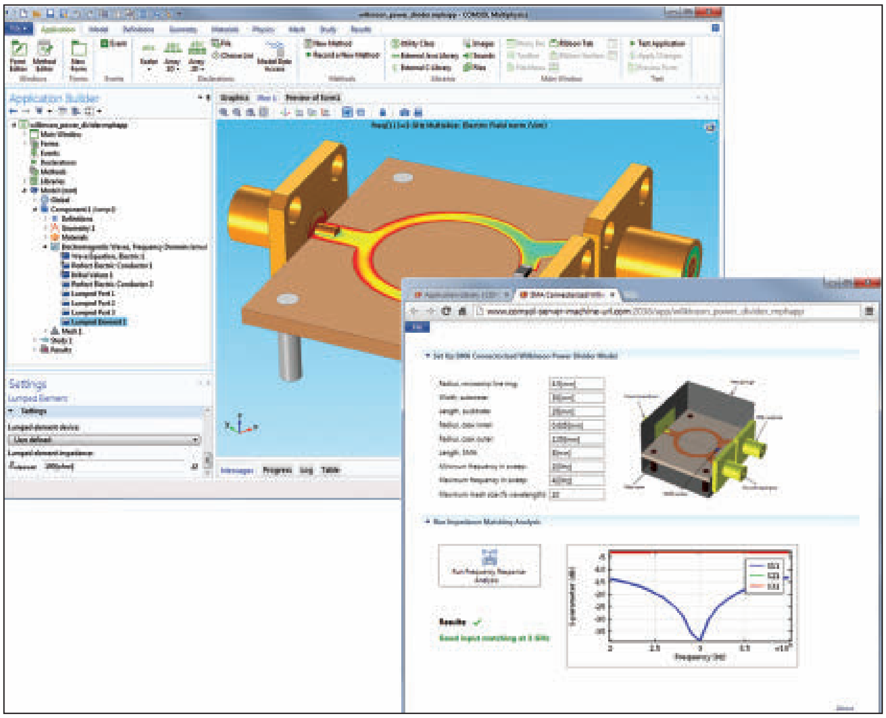

▲ *Fig. 1 The simulation of a Wilkinson power divider (upper left) is turned into an application (lower right), where the user only needs to change design parameters and run the simulation in a browser to analyze the power divider.*


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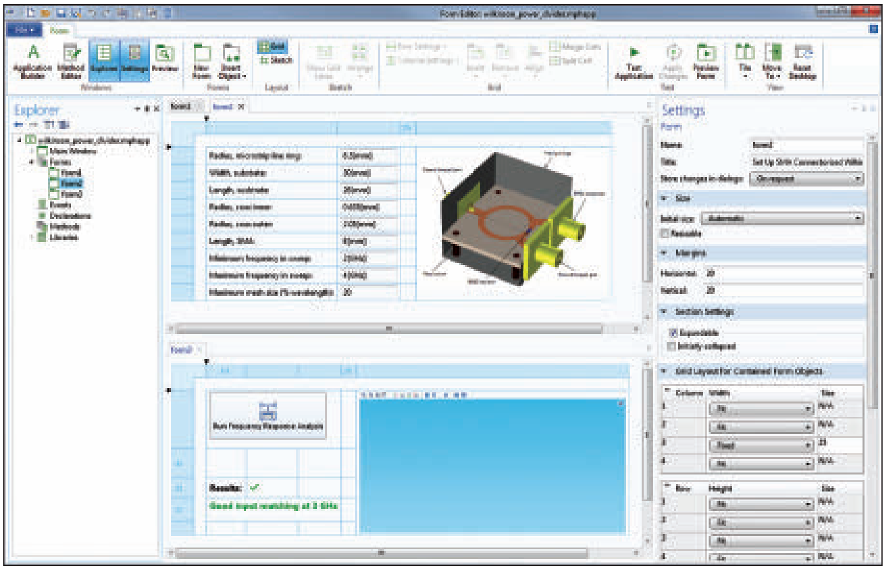


▲ *Fig. 2 The Form Editor is used to design and lay out the application interface, using form objects such as input fields, graphics and buttons.*

mechanical, fluid and chemical effects can be combined and coupled to create a simulation that accurately represents the real world from within a single graphical interface. The software offers application-specific and interfacing modules for analyzing various physics phenomena, and additional physics capabilities are included with each new release.

Version 5.0 adds three new modules to the extensive product suite: the Ray Optics Module, Design Module and LiveLink™ *for Revit*®. It also provides additional predefined multiphysics couplings, added functionality for geometry and meshing capabilities, and various new features for simulating physics phenomena.

The major new addition to COMSOL Multiphysics is the Application Builder, now included in the software's core functionality.

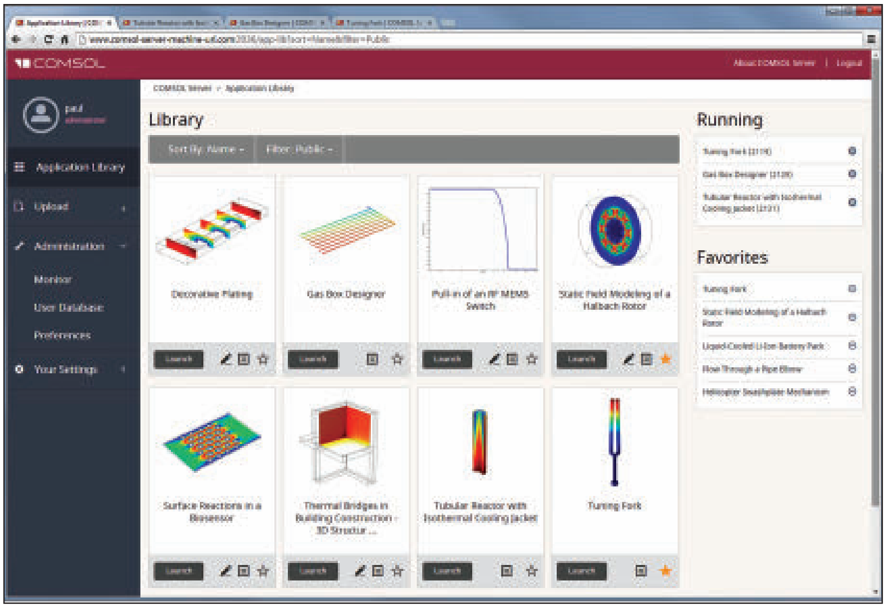
APPLICATION BUILDER AND COMSOL SERVER

The Application Builder brings multiphysics simulation to a wider audience by allowing simulation experts to build applications that can be used by engineering, manufacturing and others. With the Application Builder, engineers can create easy-to-use applications from their COMSOL multiphysics models. The Application Builder is included with the Windows version of COMSOL Multiphysics 5.0 and provides all the tools needed to build and run the apps.

After a model is finalized, the engineer who created the simulation uses the Application Builder to design a simplified user interface that displays only the parameters relevant to a specific project (see ***Figure 1***). The application is then shared with users – either within the company or externally – who can update and test new model parameters without needing to involve the designer.

The application can include user documentation, automated checks for valid inputs and predefined reports. This avoids accidental input errors and keeps the focus on the relevant output data.

The process for building an application starts with a simple command: Save Model as Application. From here, the Application Builder takes the user through the necessary steps: choosing the parameters to make available for editing, processing and presenting the results. The Form Editor (see ***Figure 2***) is used to design the user interface, through click and drag-and-drop operations, and the Method Editor is used to implement custom commands. There are no limitations to the operations that can be implemented using the Method Editor – from generating reports, playing sounds, or sending emails when the computation is complete, the designer can develop any desired command.



▲ *Fig. 3 COMSOL Server™ allows users to run simulation apps built with the Application Builder and is the hub for controlling their deployment, distribution and use.*

After creating an app with the Application Builder, COMSOL Server (see ***Figure 3***) provides an efficient and cost-effective solution for managing how the app is used. COMSOL Server is the engine for running COMSOL apps and the hub for controlling their deployment, distribution and use. Applications can be run in a COMSOL Client for Windows or in various browsers, such as Google Chrome, Firefox, Internet Explorer and Safari. COMSOL Server can be hosted in a corporate network or in the cloud.

When applications are run using a web browser, updated versions of the application can be deployed instantaneously to all users. No plug-ins are needed to run applications in a browser.

Since the release of COMSOL 5.0, the Application Builder has been adopted into the design processes of many world-renowned companies and institutions. With the click of a button, widely dispersed teams can now perform technical analysis, provide cost estimates based on customers' requirements and test different materials and design components.

Just as simulation has improved product development and shortened time to market, simulation apps can further accelerate time to market, improve accuracy in the field and improve customer service.

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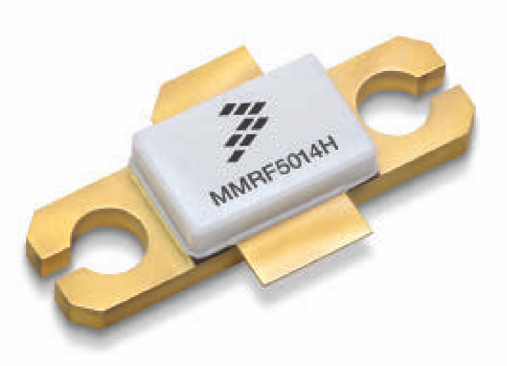


125 W GaN HEMT Covers 1 to 2700 MHz

Freescale Semiconductor
Tempe, Ariz.

The significant advantages of gallium nitride (GaN) have mostly been discussed in relation to delivering high peak power in narrowband pulsed applications, primarily active electronically scanned array (AESA) radar. However, as GaN devices are inherently broadband, they are also appealing for use in electronic warfare (EW) or applications with multiple narrow frequency bands, such as military radios. To serve these, Freescale Semiconductor has introduced the MMRF5014H, a GaN on SiC HEMT power transistor that delivers at least 125 W, CW or pulsed, up to 2700 MHz and 100 W CW from 200 to 2500 MHz.

FEATURES AND BENEFITS

A device with broad bandwidth allows designers to use a single device, rather than several, to cover an entire range of operating frequencies. Most military radios and other systems operating in the frequency range of the MMRF5014H employ silicon power transistors. While these are rugged and achieve high levels of performance, they are usually designed and matched to operate over narrow frequency bands. Consequently, a system covering an octave bandwidth requires three or four transistors, one for each segment of the frequency range. This design approach increases system complexity and cost. The MMRF5014H can be matched over a much wider frequency range, requiring fewer amplifiers and transistors – in some cases only one. Also, manufacturers can design a range of products that cover different bands from HF through S-Band using just the MMRF5014H as the output transistor.

In many applications, power amplifiers are subjected to significant impedance mismatches that can destroy power transistors. While some "high-ruggedness" LDMOS transistors can survive extreme mismatches without performance degradation or failure, this has generally not been true for GaN HEMTs, whose rated maximum VSWR is generally 2:1, and usually no greater than 5:1. The MMRF5014H is an exception, designed to deliver full CW power into a 20:1 VSWR without degradation or failure, even at twice its rated input drive. With this level of ruggedness, the MMRF5014H is well suited for battlefield radios and industrial systems such as RF heating, where significant impedance mismatches are common.

The thermal design of the system is a challenge when using a GaN power transistor, since the high power density (W/mm of gate periphery) of GaN generates greater heat concentration than other device technologies. So the thermal resistance from device junction to package base is a key parameter. It should be as low as possible to allow the heat to efficiently spread away from the device and into the heat sink. At less than 1° C/W, the MMRF5014H

has the lowest thermal resistance of any commercially available GaN HEMT. The device is housed in Freescale's NI-360H ceramic air-cavity package.

RF PERFORMANCE

Detailed specifications for the MMRF5014H are shown in ***Table 1***. In Freescale's 200 to 2500 MHz applications circuit, the power transistor achieves greater than 40 percent drain efficiency over the full frequency range and 58 percent at narrower bandwidths. Gain is greater than 12 dB and increases to 16 dB over narrower bandwidths.

Like all Freescale RF power transistors, the MMRF5014H is conservatively rated, as demonstrated in ***Figure 1***. In this pulsed radar application between 1300 and 1900 MHz, the gain, efficiency and RF output power are significantly higher than rated. This is also true over the full bandwidth of the transistor, as shown in ***Figure 2***.

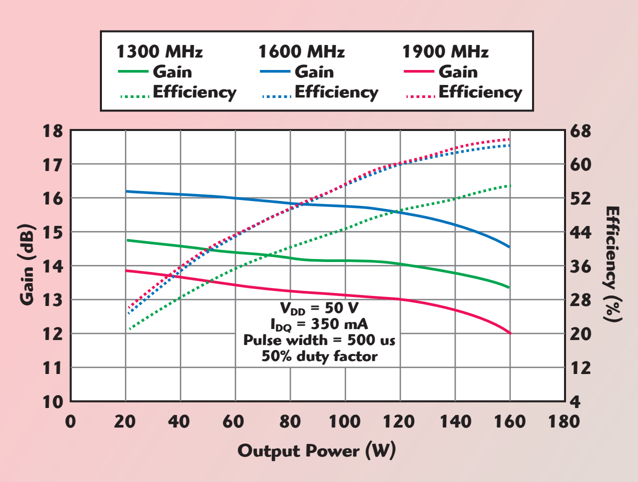
Samples and evaluation circuits for the MMRF5014H are available now. The device can be ordered on tape and reel.

Unlike the volatile wireless market, defense systems require a commitment to long-term availability, as systems remain operational for many years after being deployed. To satisfy this requirement, the MMRF5014H and all products designed for defense applications are part of Freescale's product longevity program, which guarantees availability for 15 years.

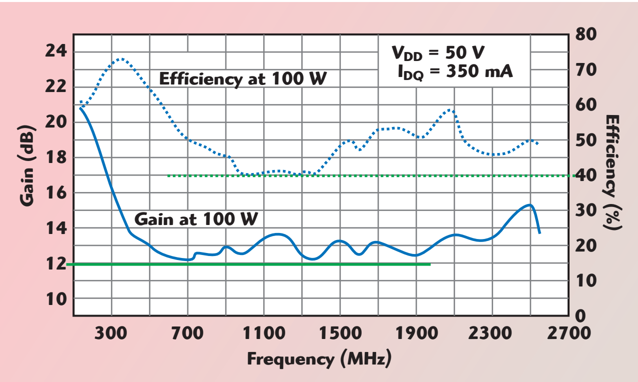
TABLE 1

KEY PERFORMANCE SPECIFICATIONS

Device Type	GaN depletion-mode HEMT, SiC substrate
Frequency Range (MHz)	1 to 2700
RF Output Power, CW or Pulsed (W)	
2500 MHz (Narrowband Test Fixture)	125 minimum
200 to 2500 MHz (Wideband Application Circuit)	100 minimum
Drain Efficiency (%)	40 to 58
Gain (dB)	12 to 16
Thermal Resistance (°C/W)	1.0
Impedance Mismatch Ruggedness	20:1, 3 dB overdrive, 50 VDC with no device degradation
Maximum Junction Temperature (°C)	+225
Package	NI-360H ceramic air-cavity



▲ *Fig. 1 Narrowband gain, efficiency and RF output power under pulsed operation.*



▲ *Fig. 2 Wideband gain and efficiency at 100 W CW output power.*

Freescale Semiconductor
Tempe, Ariz.
www.freescale.com/RFmilitary

Phase Adjusters

Part Number	Connectors	Frequency Range (GHz)	VSWR max.	Insertion Loss max. (dB)	Phase Shift min. (°)	No. of Turns	Phase Shift Deg/GHz/Turn	Time Delay min. (psec.)	Time Delay max. (psec.)	Temperature (°C)	Weight max. (g)
LS-0002-YYYY[1]	div.	DC - 2	1.2:1	0.3	85	37	1.15	393	516	-65 to +125	98-220[2]
LS-0103-6161	Nf	DC - 3	1.15:1	0.4	540	cont.		1826	2328		700
LS-0203-6161				0.9	1080			3693	4694		1200
LS-0012-YYYY[1]	div.	DC - 12	1.3:1	0.8	520	37		406	530		114-234[2]
LS-0112-XXXX[3]	SMA	DC-12.0	1.25:1	0.4	230	16.5	1.2	238	293	-65 to +125	70
LS-A112-XXXX[3]											47
LS-0212-1121											70
LS-A212-1121											47
LS-0118-XXXX[3]		DC-18.0		0.6	350						70
LS-A118-XXXX[3]											47
LS-0218-1121											70
LS-A218-1121											47
LS-0118-5161	N							300	355	-65/+70	105
LS-U118-5161										-65/+165	
LS-0018-YYYY[1]	div.	DC - 18	1.5:1	1.0	770	37	1.15	406	530		98-220[2]
LS-0121-XXXX[3]	SMA	DC-26.0	1.30:1	0.8	500	16.5	1.2	238	293	-65 to +125	70
LS-A121-XXXX[3]											47
LS-0221-1121											70
LS-A221-1121											47
LS-0321-1121			1.31:1		500	35	0.6	236.7	290.5		30
LS-0170-1121			1.26:1	0.26	127	13.5	0.36	109.2	122.8		9
LS-S008-1121			1.50:1	0.4	155	10	0.6	118.6	135.1		20
LS-P140-KFKM	2.92 mm	DC-40.0	1.2:1	0.6	590	12	1.2	168	208	-65 to +65	51
LS-0140-KFKM			1.4:1								49
LS-P150-HFHM	2.40 mm	DC-50.0	1.3:1	0.8	400	7		172	195		55
LS-0150-HFHM			1.5:1								53
LS-P165-VFVM	1.85 mm	DC-63.0	1.4:1	0.8	600	8		167	195		55
LS-0165-VFVM			1.5:1								53

1) div.: Connector Configuration available: SMA, male and female; N, male and female; TNC male and female
2) Weight depends on connector configuration
3) SMA Connector Configuration available: male/female; male/male; female/female; female/male

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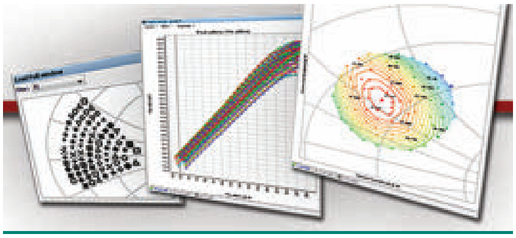
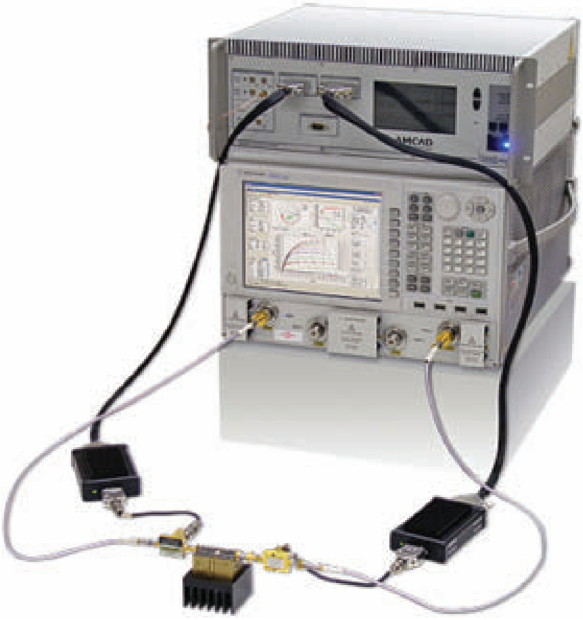
PhaseShiftersTable



IVCAD Release 3.5

Maury Microwave
Ontario, Calif.



▲ *Fig. 1 BILT/IVCAD pulsed IV/S-parameter characterization system.*

The consolidation of industry players and an overall reduction in acceptable time-to-market have led to demands for streamlined and efficient measurement and modeling device characterization tools. Maury Microwave and strategic partner AMCAD Engineering have addressed this challenge by releasing revision 3.5 of the IVCAD measurement and modeling device characterization software, the most complete commercial solution to cover the design flow from component to circuit to system.

COMPACT TRANSISTOR MODELING

The design flow begins with linear and nonlinear model extraction of popular transistor technologies, such as GaN FET and LDMOS. IVCAD, using AMCAD's BILT pulsed IV system and a pulsed network analyzer (see ***Figure 1***), measures synchronized pulsed IV and pulsed S-parameter characteristics at various gate and drain bias voltages. Pulse widths are set to eliminate self-heating and operate the transistor at quasi-isothermal conditions. The quiescent gate and drain voltages are set to isolate and model gate-lag and drain-lag trapping. Measurements can be repeated at varying chuck temperatures to extract an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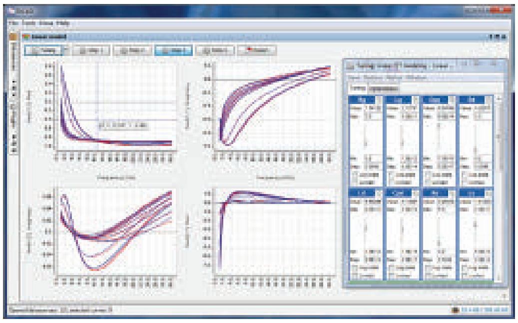


▲ *Fig. 2 Linear model extraction tool.*

electrothermal model component.

AMCAD GaN HEMT and LDMOS model extraction is performed within the IVCAD platform; the same tool used to record relevant measurements is also used to extract the complete compact model. The measured S-parameters are used to create a linear model consisting of extrinsic (i.e., pad capacitances, port metallization inductances, port ohmic resistances) and intrinsic (i.e., channel capacitances, ohmic resistances, mutual inductance, output capacitance and resistance) parameters (see ***Figure 2***). Synchronizing the pulsed IV and pulsed S-parameter measurements enables the nonlinear capacitances, voltage-controlled output current source, diodes, breakdown generator, thermal and trapping elements to be extracted.

LOAD-PULL MEASUREMENT AND MODELING

Load-pull measurement involves varying the load impedance presented to a device under test (DUT) at one or more frequencies and measuring its performance: output power at the fundamental and harmonic frequencies, gain, efficiency, and intermodulation distortion (see ***Figure 3***). Load-pull characterization supports extracting and validating models, designing amplifiers, testing performance with mismatch, and evaluating robustness.

Once a nonlinear compact model has been extracted, load-pull can refine the model by adjusting the nonlinear parameters to better match nonlinear measurements. Load-pull can also be used to validate models by overlaying the simulated and measured transistor performance as a function of the load impedance presented to the transistor.

IVCAD supports multiple forms of real time, vector network analyzer (VNA) load-pull:

- CW and pulsed
- Single and two-tone input signals
- Fundamental and harmonic impedance control of the source and load
- Passive, active and hybrid-active impedance generation techniques
- Time domain waveform nonlinear VNA (NVNA) load-pull, under DC and pulsed bias stimulus.

Passive load-pull uses mechanical impedance tuners to vary the source and load impedances presented to the DUT at the fundamental and/or harmonic frequencies. Active load-pull replaces the passive tuners at one or more frequencies with “active tuners” that use a magnitude and phase-controllable source to inject power into the output of the DUT. This creates the "reflection" signal to present the desired impedance. Active load-pull overcomes the mechanical and VSWR challenges presented by harmonic passive tuners. Hybrid-active load-pull combines the strengths of active and passive load-pull, allowing the passive tuner to act as a prematch to lower the power required by the active tuner. Combining the two also enables a "divide and conquer" approach to covering multiple frequencies.

Time-domain NVNA load-pull can record the voltage and current waveforms and load lines as well as the typical measurement parameters. This additional information conveys the sensitivity of a transistor and its class of operation.

Synchronized pulsed RF, pulsed bias load-pull uses the BILT pulsed IV system to bias the DUT for a true pulsed measurement. Pulsing the bias avoids self-heating the transistor, and it is useful for MMIC applications where the bias is pulsed.

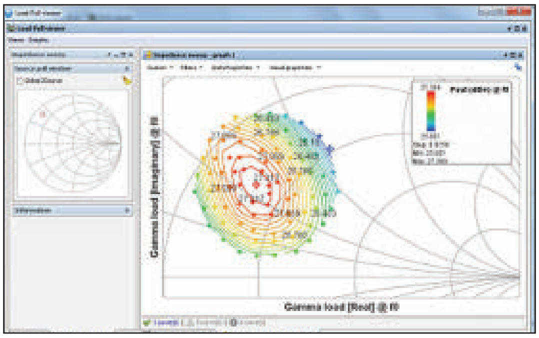
BEHAVIORAL MODELING

Behavioral modeling yields a "black-box" that models the DUT's response to a specific set of stimuli, such as input power, bias, and impedance. Compared with compact models, which completely define the characteristics of the transistor, behavioral models reflect the "behavior" and are static, meaning they are only valid under the conditions in which they were extracted. Behavioral models are useful in several applications:

- Hiding the details of the transistor and concentrating on its performance and response, which is ideal for public distribution
- Improving the speed of simulation, since behavioral models will generally simulate faster than a compact model containing the same data
- Modeling a packaged component or even a complete circuit or system, which is not compatible with compact modeling.

IVCAD supports two behavioral modeling methodologies: Keysight's X-parameters and AMCAD's Multi-Harmonic Volterra (MHV). X-parameters are the result of a polyharmonic distortion methodology (harmonic superposition), which uses harmonic extraction tones to quantify the harmonic nonlinearities of a DUT. The MHV modeling technique is based on harmonic superposition with dynamic Volterra theory, resulting in a model that handles both low and high frequency memory effects.

Behavioral modeling within IVCAD is transparent to the user. Sweep plans for impedance, power and bias are defined, and the measurement data is taken; the



▲ *Fig. 3 Load-pull contours.*

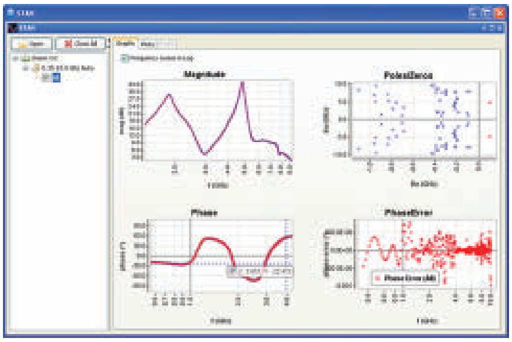


Fig. 4 MMIC stability analysis.

software communicates with the relevant model extraction application and presents a complete model following the measurement.

STABILITY ANALYSIS

Once an amplifier or integrated circuit has been designed with a circuit simulator, it is critical to test the design for both low and high frequency oscillations. IVCAD offers a Stability Analysis (STAN) module that is compatible with commercial circuit simulation tools (see ***Figure 4***). Single and multi-node analysis determines the cause and localization of oscillations. Parametric analysis identifies potential oscillations as a function of input power, bias, load impedance and stabilization network resistance. Monte Carlo analysis characterizes oscillations as a function of manufacturing dispersions and tolerances.

Whether being used for a single purpose or across multiple modeling, design and production groups, the IVCAD measurement and modeling device characterization software suite offers an intuitive, methodical and efficient set of tools to help designers achieve first-pass design success and shorten time-to-market.

Maury Microwave
Ontario, Calif.
www.maurymw.com

Remote RF Analyzer with Receiver Characteristics

The second generation of the new NRA Analyzer family comprises the 19 inch rack-mount NRA-3000-RX (9 kHz to 3 GHz) and NRA-6000-RX (9 kHz to 6 GHz) RF analyzers. Both are equipped with an RF module that has been developed for low phase noise and low intrinsic interference. The devices analyze RF signals up to 6 GHz in the frequency or time domain and simultaneously exhibit receiver characteristics, enabled by a new high frequency receiver module.

The analyzers can yield spectrums of up to 600,000 frequency points with time resolutions as fine as 30 nanoseconds. Rapid transmission of large quantities of data is possible in binary format. Unusually high channel bandwidths can be captured with the intermediate frequency bandwidth up to 32 MHz. With software, users can freely define up to 500 channels or frequency ranges to be monitored. The demodulation function makes it possible to directly hear FM, AM, USB, LSB and CW signals using external headphones.

All NRA-RX devices are 1U (1.75") high and weigh less than 5 kg. With a power consumption of less than 20 VA, they operate silently and do not require forced ventilation, making them suitable for mobile systems or confined spaces. They can also be integrated into practically any test and monitoring environment with the Ethernet interface and ASCII, plain text remote control commands. A 10 MHz reference input is provided for synchronization to the system frequency; stand-alone operation with a PC is also possible.

The devices are primarily designed for use in automated and remote controlled measuring systems. They are particularly suitable for radio surveillance and monitoring, demodulation and decoding, spectrum occupancy, coverage, signal analysis and classification, detection of illegal transmitters and SIGINT (COMINT and ELINT).

Narda Safety Test Solutions GmbH
Pfullingen, Germany
info.narda-de@L-3com.com
www.narda-nra.com

Power Over Ethernet Control for Coax Switches

Ducommun has introduced multi-throw coaxial switches that can be controlled and powered using Power over Ethernet (PoE). This option is available with a range of Ducommun products from SP3T to 6T, covering DC to 40 GHz. Since the switch is powered through the Ethernet connection, no external power supply is needed. The PoE interface provides a unique, configurable IP address, and the switch can be controlled remotely from a Windows PC (32 or 64 bit) as well as Android and iOS smartphone apps.

PoE control is useful in a wide variety of applications, including test equipment, control systems and general lab work. Several switches can be configured into a switch matrix using a single Ethernet hub.

Up to 10 GHz, the bidirectional switch has less than 0.4 dB insertion loss, greater than 60 dB isolation, and better than 1.4:1 VSWR. Switching time, including the command, is within 100 msec. Control functionality is available with failsafe and normally open modes. The operating temperature range is -35° to +85°C, and the operating life is greater than 1,000,000 throws. The cylindrical design is 1.5 inch in diameter and 7 inches tall, with a standard RJ45 connection for the PoE interface.

Ducommun,
Carson, Calif.,
www.ducommun.com

Multi-Band Antenna for Data Links

The FRF-229 multi-band panel antenna offers high performance for data links in L-, S-, C- and Ku-Bands, aligning with modern multiband radio terminals. The antenna apertures and RF amplification for all bands are contained within a single air-cooled housing that enables simple platform integration. This scalable antenna system can be configured as one to four distributed antennas working in concert to suit any installation. The L-, S-, C- and Ku-Band functions within the antenna are independent, allowing different simultaneous waveforms and data rates between the high and low frequencies. The conformal installation allows a wide field of view from a single antenna or 360° coverage with multiple antennas.

The Ku-Band function features integrated phased arrays capable of full duplex operation in the tactical common data link frequency bands, which can be reconfigured on the fly for air-to-ground, air-to-air or ground-to-ground data links. The Ku-Band phased array enables electronic elevation beam steering to compensate for the motion of dynamic platforms.

By incorporating amplification within the antenna, cable losses between the radio and antennas are offset, which improves transmitter efficiency and receiver sensitivity. This increases system performance compared to traditional antennas, while simultaneously reducing weight and DC power consumption. Built-in diplexing enables multiple frequencies to be combined onto common cables, which simplifies the installation.

Prototype systems have been flight tested under operational conditions; the production design and full MIL-STD qualification are planned during 2015.

FIRST RF Corp.
Boulder, Colo.
www.firstrf.com

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Innovations in EDA
Understanding 5G and How to Navigate Multiple Physical Layer Proposals
Presented by: Keysight Technologies
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Tips and Techniques for Making Microwave Vector Network Analysis Measurements in the Field
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Live webcast: 2/18/15

Technical Education Training
RF and Microwave Heating with COMSOL Multiphysics
Presented by: COMSOL
Live webcast: 2/19/15

RF and Microwave Education Series
Understanding Available Measurement Techniques or Unknown Signals
Presented by: Keysight Technologies
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Technical Education Training Series
- Laser Test of RIN, Linewidth and Optical Noise Parameters
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- Non-Destructive Testing of Powders, Ceramic, Oils and Other Composite Materials
- Design Challenges for Handset Power Amplifiers Due to LTE-Advanced
- RF PCB Design, Inclusive of EM Analysis
- Essential Thermal Mechanical Concepts Needed in Today's Microwave Circuit Designs
- VCO Fundamentals
- Single Sweep 70 kHz to 145 GHz Broadband System and On-Wafer Measurements
- High Frequency Materials and Characterization up to Millimeter Wave Frequencies
- Simulations of Gyrotrons with VSim
- Practical Simulation and Design of Broadband GaN RF Power Amplifiers – How Close are We to Right First Time Now?
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- Simulation of Accelerator Components
- Designing Clean Mobile Devices – Mobile Phones & Automobile Systems
- Power Delivery Network (PDN) Analysis
- Multiphysics Simulation for Medical Applications

Innovations in EDA
Presented by: Keysight Technologies
- RF System Design, Prototype & Production with X-Parameters in One Pass
- DynaFET: Advanced Model for GaN/GaAs HEMTs from NVNA Measurements and ANNs

Keysight in LTE/Wireless Series
- LTE-Advanced: 3GPP Release 12 and 13
- Characterization and Test Challenges for MMPAs with ET & DPD

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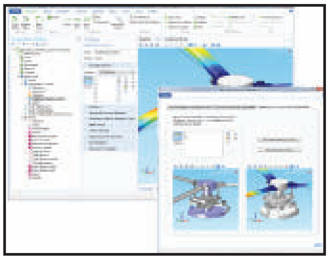


COMSOL Inc. released COMSOL Multiphysics® software version 5.0, featuring extensive product updates, three new add-on products and the new Application Builder. COMSOL users can now build applications for use by engineering and manufacturing departments, expanding accessibility to their expertise and cutting-edge simulation solutions. In addition, COMSOL® Server is a new product developed specifically for running applications built with the Application Builder. COMSOL Server enables the distribution of applications, allowing design teams, production departments and others to share applications throughout an organization using a Windows®-native client or other major web browser.

COMSOL Inc.
www.comsol.com

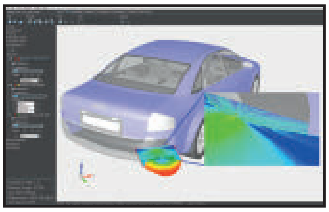
RF Assembly Calculator

VENDORVIEW

The iPhone App 'RF Tools' from HUBER+SUHNER AG has been enhanced with the assembly calculator. This useful extension provides an easy comparison of up to three HUBER+SUHNER radio frequency cables and assemblies in different configurations and environments. It offers straight access to technical specifications such as insertion loss and power rating. RF specific values such as impedance, wavelength, return loss (VSWR) and signal delay can be easily calculated on an iPhone. This app is available for free in English and Chinese in the app store.

HUBER+SUHNER AG
www.hubersuhner.com

EMPIRE XPU

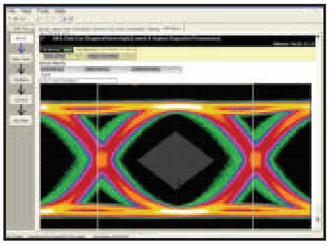


EMPIRE XPU is a 3D EM tool using finite difference time domain for antennas, RF and microwave circuits, EM chip design and more. The new version of EMPIRE features a completely redesigned graphical user interface with an updated arrangement of menus, navigation tree, toolbars and icons to ensure an intuitive simulation workflow. EMPIRE XPU is optimized to process huge amounts of imported CAD data, i.e., files larger than 2 GB, and can be imported in less than two minutes.

IMST GmbH
www.imst.com

Compliance Test Software

VENDORVIEW



Keysight Technologies introduced compliance test software for the latest Mobile High-Definition Link (MHL) specification. The MHL 3 source compliance test software allows engineers to test their MHL 3 transmitters the same way they are tested at authorized MHL compliance test centers using Keysight Infiniium oscilloscopes. The MHL 3 specification offers a significant increase in bandwidth (up to 6 Gbps) and a new bidirectional, high speed communication path between the portable device and a display. Keysight's software includes test suites for all previous versions of MHL, cable model and equalizer setup, user-defined mask setup, DUT automation control, saved waveform analysis, user comments for detailed test reports and calibration test suites.

Keysight Technologies Inc.
www.keysight.com.

LabVIEW Communications

VENDORVIEW

National Instruments introduced the LabVIEW Communications System Design Suite, which combines software defined radio (SDR) hardware with a comprehensive software design flow to help engineers prototype 5G systems. The LabVIEW Communications environment enables a design team to map an idea from algorithm to FPGA using a single high-level representation. It includes built-in application frameworks for Wi-Fi and LTE that enable wireless prototypers to focus on innovating specific components of existing standards rather than designing a new algorithm from scratch. LabVIEW Communications helps bridge the gap between the ongoing rollout of 4G and the to-be-determined 5G standards of the future.

National Instruments
www.ni.com/labview-communications

Wavelength Calculator on ROG Mobile

VENDORVIEW

The new wavelength calculator on the ROG Mobile app makes it easy for designers to calculate electrical length, phase delay and wavelength fractions when evaluating a high frequency circuit material with a specified dielectric constant (Dk). It also allows comparisons of two materials with different Dk values and displays differences in wavelength fractions as well as potential size reduction of circuit features. ROG Mobile is available for free download for Apple and Android devices.

Rogers Corp.
www.rogerscorp.com

New Waves

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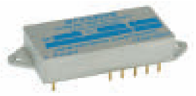
Components

50 W DC-DC Converter

VENDORVIEW



Crane Aerospace & Electronics introduced its Interpoint® MFX Series™ 50 W DC-DC converter. The newly designed MFX Series provides up to 50 W in a 0.92 cubic inch case with efficiency over 90%. The input voltage of 16 to 50 V can also withstand transients of 80 V for one second, has ±10% trimmable 3.3 and 5 V outputs and operates -55° to +125°C.

Crane Aerospace & Electronics
www.craneae.com

PIN Diodes

The Eclipse EGP7000 series of PIN diodes are processed with a high resistivity epi that have intrinsic layers ranging in thickness from 4 to 200 micron depending on performance specifications. These diodes are made with a grown junction P++ layer that yields abrupt junction structures that provide low punch through voltages and minimize autodoping. They are available as chips or in your choice of 19 packages.

Eclipse Microwave
www.eclipsemicrowave.com

Wideband Power Dividers

Model D-1050-2 is a two-way power divider spanning 10 to 50 GHz. The maximum insertion loss is less than 1.8 dB. Amplitude balance is 0.5 dB maximum and phase balance is 5 degrees maximum. The minimum isolation is 16 dB and VSWR is 1.70:1 maximum. Connectors are 2.4 mm female. Housing size is 1.15" × 1.06" × 0.5".

Electromagnetic Technologies Industries Inc.
www.etiworld.com

PIN Diode Phase Invariant Attenuator

Model A6P-78N-0JM is a phase invariant digitally controlled PIN diode attenuator that operates from 8 to 18 GHz. It is capable of 64 dB range in monotonic 0.0625 dB steps. The attenuation flatness is ±3.5 dB and the delta phase is ±18 degrees at 64 dB. With a maximum VSWR of 2.0:1 and an insertion loss less than 7.5 dB, it accommodates a supply voltage of +15 VDC at 30 mA, -15 VDC at 125 mA and +5 VDC at 100 mA.

G. T. Microwave Inc.
www.gtmicrowave.com

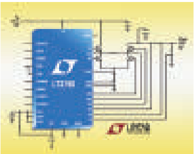
Miniature SMT Highpass Filter

Integrated Microwave Corp. offers a highpass filter in a unique miniature SMT housing with a -3 dBa cutoff frequency of 1800 MHz, a -0.5 dBa passband of 1900 MHz and a stopband of greater than 45 dBc from DC to 1000 MHz. This unit measures 0.80" × 0.44" × 0.33".

Integrated Microwave Corp.
www.imcsd.com

60 V, Synchronous Buck-Boost Controller

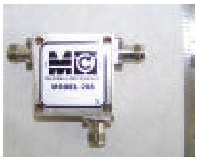
VENDORVIEW



Linear Technology announced the LT3790, a synchronous buck-boost DC/DC controller that delivers up to 250 W of power with a single IC. Its 4.7 to 60 V input voltage range makes it ideal for a wide variety of automotive and industrial applications. Its output voltage can be set from 0 to 60 V, making it well suited as a voltage regulator or battery/supercapacitor charger. The LT3790's unique design utilizes three control loops to monitor input current, output current and output voltage to deliver optimal performance and reliability.

Linear Technology
www.linear.com

High Power Circulator



Model 288 is a high power circulator that operates from 118 to 174 MHz and offers continuous forward power of 200 W (internal load rated at 50 W CW). The M288 delivers a max. VSWR of 1.35 : 1 with isolation of 17 dB or more and insertion loss under 0.7 dB. The operating temperature range is 0° to +55°C (with capacity to withstand a non-operating temperature range of -40° to +85° C). The M288 is only 2" × 2" × 0.75".

McManus Microwave
www.mcmanusmicrowave.com

Ceramic Capacitors

Passive Plus Inc. has introduced the 01005BB104 and 0201BB104 ultra-broadband 100 nF multilayer ceramic capacitors. The 01005BB104, the industry's smallest 100 nF broadband part characterized for RF performance, has a case measuring (mils) 16 × 8 × 8, and offers resonant-free RF coupling/DC blocking from 16 KHz (lower 3 dB frequency) to beyond 65 GHz with < 1 dB insertion loss and < -15 dB return loss on suitable substrates.

Passive Plus Inc.
www.passiveplus.com

Digital Phase Shifter

VENDORVIEW

PMI model no. PS-360-DC-IR-9G11G is a 9 to 11 GHz, digitally controlled analog phase shifter with capability for phase shifting from 0° to 360°.

Planar Monolithics Industries Inc.
www.pmi-rf.com

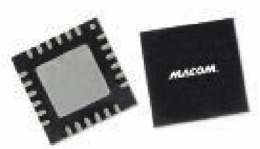
Two-way Power Divider

Pulsar is racing towards 100 GHz. The latest in its standard lineup is a two-way power divider, Model PS2-57-450/15S covering a frequency range of 10 to 70 GHz with 2 dB of insertion loss and 12 dB isolation. Amplitude balance is ±1 dB and phase balance is ±10 degrees. Outline dimensions are 1.0" × 0.8" × 0.38" with 1.85 mm female connectors.

Pulsar Microwave Corp.
www.pulsarmicrowave.com

Integrated Up-Converter

VENDORVIEW



Richardson RFPD Inc. announced the availability and full design support capabilities for a new up-converter from M/A-COM Technology Solutions. The MAUC-011003 is an integrated up-converter assembled in a lead-free 4 mm 24-lead PQFN plastic package. It features a typical conversion gain of 12 dB, image rejection of 15 dBc, and is integrated with an LO doubler, LO buffer amplifier and RF buffer amplifier. Operating over the 27.5 to 33.4 GHz frequency bandwidth, the device offers high LO suppression that eliminates the need for a Tx filter.

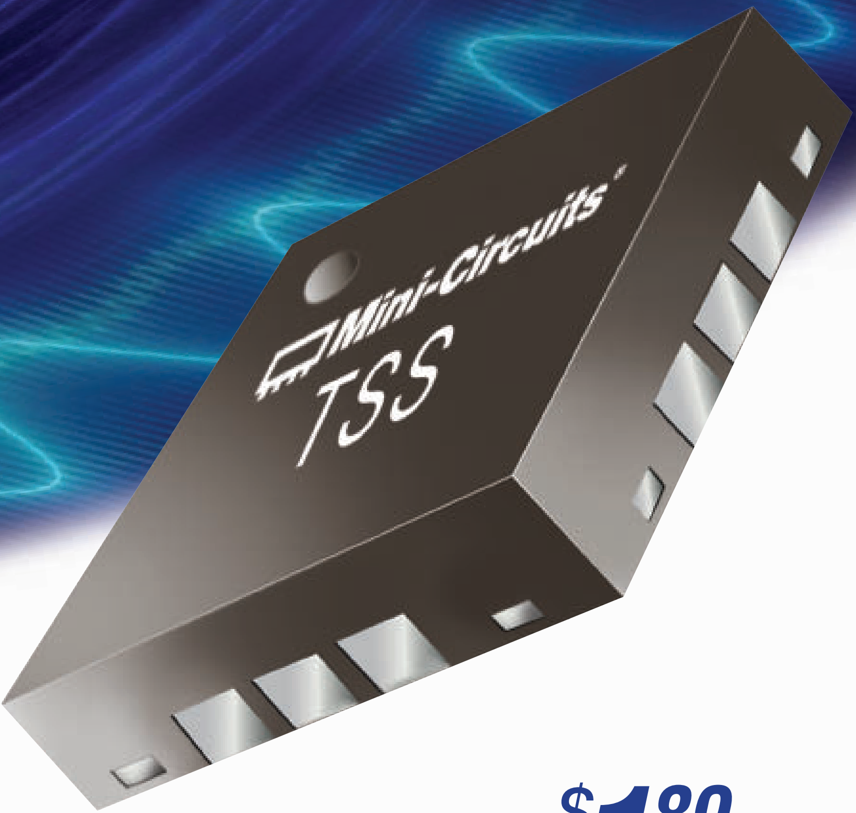
Richardson RFPD
www.richardsonrfpd.com

High Power SPDT Switch

RLC Electronics announced the addition of a high power 18 GHz SPDT switch with N connectors to its product capabilities. The switch can handle 1000 W at 100 MHz, 200 W at 4 GHz and 125 W at 18 GHz, and provides high reliability, long life and excellent electrical performance characteristics over the frequency range (including high isolation). Options on the switch include operating mode (failsafe or latching) and coil voltage (12 or 28 VDC), as well as indicator circuitry and a TTL driver.

RLC Electronics Inc.
www.rlcelectronics.com

LOW NOISE BYPASS AMPLIFIERS



500 MHz-5 GHz

$1.89 from ea.(qty.1000)

Very rarely does a new product achieve many breakthrough features in one model. Mini-Circuits' TSS-53LNB+ is this rare exception. With ultra-wide frequency range and excellent gain flatness, this revolutionary amplifier is ideal for broadband and multi-band applications from military and commercial wireless to instrumentation and more! Its integrated, switchable bypass circuit allows you to protect the LNA in the presence of large signals and extend the usable dynamic range – all in a tiny, 3x3mm package! Visit minicircuits.com for full specs and off-the-shelf availability for delivery as soon as tomorrow!

- *21 dB Gain in LNA Mode*
- *Ultra Flat Gain, ±1.5 dB from 500 to 3500 MHz*
- *Internal Bypass Switch for Large Signals*
- *Low Noise, 1.4 dB*
- *+21 dBm Output Power*
- *+34 dBm IP3 in LNA Mode*
- *+50 dBm IP3 in Bypass Mode*
- *Tiny Size, 3x3mm*

RoHS compliant.

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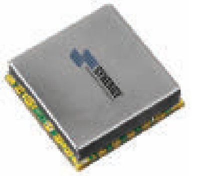
www.minicircuits.com P.O. Box 350166, Brooklyn, NY 11235-0003 (718) 934-4500 sales@minicircuits.com

525 rev A

Four-Port Bi-Directional Coupler



MFSH615712-100 is a miniature intelligent interactive synthesizer that operates from 6150 to 7120 MHz with a 1 MHz step size in a 0.6" × 0.6" × 0.175" (L × W × H) RoHS size surface mount package. Features include an on-board micro-controller for simplified communication, 0 dBm minimum output power, 25 dB typical harmonic suppression, 60 dB spurious suppression and a low phase noise performance with an external 10 MHz reference applied over an operating temperature range of -40° to -85°C.

Synergy Microwave Corp.
www.synergymwave.com

EPCOS SAW Duplexer

TDK Corp. announced the new EPCOS duplexer for LTE Band 1, which at 60 dB features very high isolation for both the Tx and Rx paths. Based on SAW technology, the B8651 duplexer has a miniature footprint of just 1.8 × 1.4 mm. Based on good separation of the Tx and Rx signals, the new EPCOS duplexer can be combined with power-saving envelope tracking power amplifiers without any additional prefiltering. This significantly simplifies design of the front-end, leading to major cost benefits.

TDK Corp.
www.tdk.com

Latching Multi-Throw CCR-39 SP10T Coaxial Switch

Teledyne coax switches introduced its new Series CCR-39 coax switch. The CCR-39 is a broadband multi-throw, electromechanical coaxial switch designed to switch a microwave signal from a common input to any of 10 outputs. The CCR-39 latching switch covers DC to 10 GHz and is available with 12, 15, 24 and 28 coil voltages. The CCR-39 has a characteristic impedance of 50 Ohms and an individual latching actuator allowing random position selection and minimal switching time.

Teledyne Coax Switches
www.teledyne.com

Cables and Connectors

4.1/9.5 (mini DIN) Terminations

VENDORVIEW

MECA now offers 4.1/9.5 (mini DIN) male and female terminations with power ratings of 1 and 10 W (2 kW peak) in frequencies from Hz to 3 GHz. The TMDM1-3 is the mini DIN-male, and the TMDF1-3 is the mini DIN-female.

MECA Electronics Inc.
www.e-meca.com

Type N R/A Adaptors

Response Microwave, Inc. announced the availability of its new precision Type N right angle in-series adaptors for use in test and instrumentation applications. The new RMAD.IS.N18mfRA covers DC to 18 GHz offering max. VSWR of 1.25:1 with N female to N male connector interfaces. The unit has low loss and mechanical package is 1.75" × 1.80". Material is SU303F stainless with passivate finish. The male nut is a combo hex/knurl for mating via hand or torque wrench.

Response Microwave Inc.
www.responsemicrowave.com

QuarterBack Connector Series

SV Microwave released their new QuarterBack® series of SMP/SMPM connectors. The line utilizes a quarter turn bayonet style coupling nut with a locking feature for standard SMP/SMPM interfaces. The QuarterBack® connectors are ideal for high vibration and test applications that require a large number of mating cycles.

SV Microwave
www.svmicrowave.com

NewProducts

Amplifiers

Solid-State Hybrid Power Amplifier

VENDORVIEW

Model 50HM1G6AB-47 is a compact, wideband, 50 W Class AB solid-state hybrid power amplifier module that instantaneously covers 1 to 6 GHz. It operates from a single DC voltage and provides 48 dB of typical gain with excellent gain flatness, noise figure and low intermodulation distortion for military and wireless applications.

AR RF/Microwave Instrumentation
www.arworld.us

Low Noise GaN Amplifier

VENDORVIEW

Custom MMIC announced the release of the CMD218, a 5 to 9 GHz low noise amplifier (LNA) in die form, to its growing line of standard GaN products. The CMD218 offers a gain of 22 dB, output of 1 dB, compression point of +19.5 dBm and noise figure of less than 1.25 dB across 5 to 9 GHz. In addition, without an input limiter, the CMD218 can survive high incident power levels up to 5 W with no degradation in performance.

Custom MMIC
www.custommmic.com

Sources

900 to 940 MHz VCO

Crystek's CVCO33CL-0900-0940 VCO operates from 900 to 940 MHz with a control voltage range of 0.2 to 2 V. This VCO features a typical phase noise of -104 dBc/Hz at 10 KHz offset and has excellent linearity. Output power is typically +3 dBm. Engineered and manufactured in the U.S., this new VCO is packaged in the industry standard 0.3" × 0.3" SMD package. Input voltage is 3 V, with a max. current consumption of 20 mA. Pulling and pushing are minimized to 8 MHz and 1 MHz/V, respectively.

Crystek Corp.
www.crystek.com

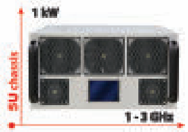
Microwave Power Modules

In many military applications, stringent requirements for size and weight must be met without sacrificing power performance. These high-efficiency, conduction-cooled microwave power modules (MPM) provide extremely dense packaging across 2 to 40 GHz. dB Control's MPMs are based on a modular design for easy customization and are available with continuous wave or pulsed power. Each MPM is a complete microwave amplifier that uses both traveling wave tubes and solid-state technologies.

dB Control
www.dbcontrol.com

1 to 3 GHz, 1 kW HPA in 5U Chassis

VENDORVIEW



Model 2170, covering 1 to 3 GHz and delivering 1 kW of broadband output power in a 5U, air cooled chassis is Empower RF Systems' latest market release. Offering unrivaled size/power advantages and building on a design architecture that has been a catalyst for technology upgrades from customers with diverse requirements from multiple markets, model 2170 provides excellent performance for end applications that include, but are not limited to, test and measurement, electronic warfare and communications.

Empower RF Systems Inc.
www.empowerrf.com

Wideband 4 W Amplifiers

VENDORVIEW

With 4 W output power and ±1 dB gain flatness across 500 to 4200 MHz, Mini-Circuits' new ZHL-4W-422+ Class A amplifiers meet your needs for a wide range of applications. With

NewProducts

rugged construction and extensive built-in safety features, they are perfect for lab uses such as production test, burn in, life test and IP3 measurements where filtering and attenuation matching is needed. Used in conjunction with Mini-Circuits' power splitters, they can be used to drive up to 32 simultaneous channels or more, improving test efficiency and throughput.

Mini-Circuits
www.minicircuits.com

35 W L-Band Power Amplifier

NuWaves Engineering introduced the next generation of its NuPower™ small, lightweight and high-efficiency power amplifier family of products with the NuPower 13G05A. The NuPower 13G05A provides saturated RF power of at least 35 W from 800 to 2000 MHz with greater than 40% module efficiency across the frequency band. With a nominal input drive level of 0 dBm, the NuPower 13G05A offers an impressive 45 dB of RF gain.

NuWaves Engineering
www.nuwaves.com

High Power Linear RF Amplifiers

VENDORVIEW

Pasternack Enterprises Inc. announced the release of eight new high power linear amplifiers that provide accurate signal amplification across a multitude of commercial and defense applications such as communications, radar and sensors, test instrumentation, telecom infrastructure, fixed microwave backhaul and commercial two-way radio. These GaAs PHEMT MMIC-based amplifiers operate from 0.8 to 9.5 GHz and can be used as high power output amplifiers or driver amplifiers depending upon the system architecture.

Pasternack Enterprises Inc.
www.pasternack.com

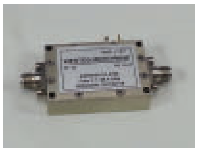
Low Noise Amplifier

VENDORVIEW

Model SBL-0524034260-KFKF-SB is a benchtop broadband low noise amplifier operating from 0.5 to 40 GHz. The amplifier exhibits 42 dB small signal gain and average 6 dB noise figure over the entire frequency range. The minimum P-1 is +10 dBm. The bench top amplifier is designed to use 100 to 240 V AC power directly from lab outlet. The bench top amplifier measures 3.75" (W) × 4.15" (L) and 1.75" (H). It is equipped with K female connectors for RF input and output connections.

SAGE Millimeter Inc.
www.sagemillimeter.com

Broadband Power Amplifier



Model ABP2650-01-2725 is a MMIC based power amplifier offering 27 dB of linear gain and 25 dBm typical output power at 1 dB gain compression point over the frequency range from 0.1 to 26.5 GHz with excellent gain flatness and VSWR. The amplifier has built-in DC voltage regulator and requires a single +12 V DC power supply. The package size of the amplifier is 1.5" × 1.0" × 0.4".

Wenteq Microwave
www.wenteq.com

Fixed Frequency Synthesizer

Z-Communications Inc. announced a new RoHS compliant fixed frequency synthesizer. Model SFS13050H-LF is a single frequency synthesizer that operates at 13.05 GHz with an external 100 MHz reference oscillator. Featuring a typical phase noise of -88 dBc/Hz at 10 kHz offset makes it an ideal choice for radar systems requiring superior performance. SFS13050H-LF is designed to deliver an output power of 0±3 dBm while operating over the industrial temperature range of -40° to 85°C.

Z-Communications Inc.
www.zcomm.com

Systems

Telematics System for M2M

RoTrack-GPS-1000 is an autonomous telematics system for positioning, tracking and sensing objects that have applications in the M2M, IoT and industry 4.0 sectors. It is an energy autarkic telematics system powered by an internal off-the-shelf battery. With an IP 65 housing, it can accommodate up to 4,000 data positions in internal storage if transmission via GSM-net is not available. It features a web portal for localization, dispatching and asset monitoring in real time.

Rosenberger Hochfrequenztechnik GmbH & Co. KG
www.rosenberger.com

Antennas

Magnetic Tracking Antennas

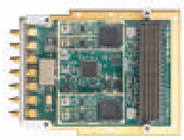
Available in five different versions – two passive and three active – the MDF series of magnetic tracking antennas covers 9 kHz to 400 MHz. By utilizing these antennas, regular spectrum analyzers can become professional field strength meters with tracking

function in a few simple steps. Due to the high directionality of the antenna, the MDF is suitable for signal direction finding. It can therefore be used as a signal direction finder or for locating illegal or unwanted interference sources.

Aaronia AG
www.aaronia.com

Test Equipment

FMC I/O Module



Innovative Integration's new FMC-1000 is a high speed digitizing and signal generation FMC I/O module featuring two, 1250 MSPS A/D channels and two 2500 MSPS D/A channels supported by sample clock and triggering features. Power consumption is 13 W for typical operation and may be conduction cooled. This FMC-1000 is the bedrock for applications such as wireless receiver and transmitter, LTE, WiMAX physical layer, RADAR, medical imaging and high speed data recording and playback.

Innovative Integration
www.innovative-dsp.com

MPI TITAN™ Probes

MPI Corp. announced its next generation of RF probe line. The TITAN™ probes feature patented protrusion tip design and matched 50 Ohm MEMS contact tips. The high-power model enables testing of active/passive RF high power devices at 10 W of continuous power, DC currents up to 2 A, bias voltages up to 250 V and at the temperature range from -60° to +200° C. Available in single-ended and dual tip configurations with pitch from 50 to 1250 micron and 26 to 110 GHz.

MPI Corp.
www.mpi-corporation.com

MICRO-ADS

Introduction to Communication Networks

Tarmo Anttalainen and Ville Jääskeläinen

Reviewed by: Gary Lerude

In the late 90s, when I became deeply involved in commercial markets for GaAs MMICs, I found a book that helped me understand many of the applications my company was targeting. "Residential Broadband," written by George Abe and published by Cisco Press, was an excellent technical tutorial. It described the system architectures and technical trade-offs, and provided insight into the system-level concerns driving the component requirements.

In the ensuing 15 years, we've seen close to a revolution in broadband communication technology, both wired and wireless. Data rates and consumption have exploded, we expect to be connected anywhere and all the time, and the networks enabling this have been transformed, gradually merging into a single global IP network for data, voice and video. Although my copy of "Residential Broadband" still sits on my bookshelf, it's no longer a reliable guide to communication technology. Fortunately, I've found a replacement.

The third edition of "Introduction to Communication Networks," recently published, provides an up-to-date explanation of the inner workings of the networks that respond to our clicks and taps. The authors describe their first purpose as making the complexity accessible to the student or a newcomer entering the field. They also want the material to inform technical professionals familiar with one area (CATV, for example) but not another (mobile phones). They avoid comprehensive mathematics by addressing the underlying theory in an easy-to-read discussion.

The material is organized into nine chapters, with problems at the end of each to test comprehension. The authors begin with an overview of telecommunications by providing a working definition and discussing the history, impact on society and the standards bodies that define the technical foundation for the services.

The second chapter covers networks and their architectures, including circuit-switched and packet. Subsequent chapters address the principles of digital communications; signals carried over the network; transmission; local area networks (LAN), both wired and wireless; Internet protocol (IP); fixed access technologies, including digital subscriber lines (DSL), cable TV and fiber to the home (FTTH); and mobile networks, including cellular, professional mobile radio (PMR) and mobile satellite systems (MSS).

Both authors teach telecommunications at Metropolia, University of Applied Sciences, in Finland. Not surprisingly, both gained practical experience working at Nokia. Ville Jääskeläinen also served as a research engineer in radar technology at the Technical Research Center of Finland.

I recommend the book for technical, marketing and sales professionals who want to expand their knowledge of telecommunications systems. Even if you don't intend to read it from cover to cover, the book is a helpful reference to keep close to your desk.

To order this book, contact:

Artech House
685 Canton Street
Norwood, Mass.
www.artechhouse.com

388 pages, $159 for print or eBook
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The 2015 IEEE International Conference on Microwaves, Communications, Antennas, and Electronic Systems

2–4 November 2015, David Intercontinental Hotel, Tel Aviv, Israel

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Call for Papers

IEEE COMCAS2015 continues the COMCAS tradition as a multidisciplinary forum for the exchange of ideas, research results, and industry experience in the areas of microwave/RF/mm-wave engineering, communications, antennas, solid state circuits, electromagnetic compatibility, engineering in medicine, electron devices, radar and electronic systems. It includes a technical program, industry exhibits, and invited talks by international experts in key topical areas.

CONFERENCE DATES: 2–4 November 2015.
CONFERENCE LOCATION: Tel Aviv, Israel at the David Intercontinental Hotel on the Mediterranean Sea.

Papers are solicited in a wide range of topics, including:

- Aeronautical and space applications and challenges Analog/digital RF circuits and systems
- Antennas (components, modeling, micro & macro scale)
- Automotive and transportation radar and communications
- Biomedical applications (body area systems, scanning devices, telemedicine)
- CAD techniques for microwave and communications devices
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- Cognitive radio and spectral sharing technologies Electromagnetic compatibility
- Fifth generation mobile communication
- Filters and Multiplexers
- First responder and military communication, sensing and information retrieval systems
- Environmentally sensitive design ("green" communications, electromagnetic, and antenna systems)
- MEMS modeling, devices and applications
- Microcell, picocell and femtocell devices, systems and applications
- Microwave and millimeter wave circuits and technologies
- Microwave imaging and tomography
- MIMO (multiple antenna systems for communications and radar)
- Modulation and signal processing technologies
- Nanotechnologies and applications
- Optical/wireless convergence and integration; radio over fiber
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- RFID devices, technologies, systems and applications
- RF power amplifiers and devices
- Sensor networks and technologies
- Software-defined radio and multiple air interface devices
- Solid-state devices, RFICs
- Spatial coding
- Terahertz technologies and systems

Submission of Abstracts

Regular oral presentations will be 20 min. in length; there will also be Poster sessions. All submitted papers will be peer reviewed and assessed on key accomplishments, technical contribution, and advancement of the state-of-the-art, originality and interest to the attendees. Accepted papers will be published in the COMCAS2015 Proceedings, which will be submitted for publication in IEEE Xplore® after the conference. For further information, see www.comcas.org.

Important Deadlines

Submission of abstract:	30 May 2015
Notification of acceptance/rejection:	15 July 2015
Submission of final camera-ready paper:	20 September 2015
Early bird (lower cost) registration:	30 August 2015

Technical Exhibition

The technical program will be complemented with a technical exhibition, which will be held on 2–3 November 2015, offering companies and agencies a unique opportunity to visit Israel and present related products and services in display and printed advertisement. For further details please contact the Conference Secretariat.

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STEM Works

Printed Circuit Board (PCB) Laminate

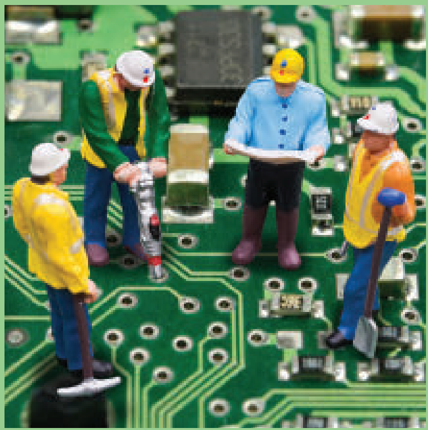
A planar structure composed of thin metallic (electrically conductive) layers bonded to insulating layers, which may be polymer, glass, ceramic or polymer filled with glass or ceramic. The PCB provides CTE-matched mechanical support for mounting electronic components and, when suitably patterned, provides conductive pathways enabling the construction of small, yet complex, reproducible and efficient circuits. The architecture lends itself to the application of high volume photolithographic board processing and pick-and-place circuit assembly for reduced manufacturing costs.

1903 German inventor Albert Hanson describes the concept of multiple-layer flat foil conductors laminated to an insulating board.

1913 A patent for a print-and-etch fabrication method (subtractive process) is granted to Arthur Berry in the U.K.

1918 Max Schoop is awarded a patent in the U.S. for an additive process, a method of flame-spraying metal onto a board though a patterned mask.

1936 Austrian engineer Paul Eisler, considered by some to be the father of the printed circuit – as we know it today – invents the PCB using photolithographic techniques as part of a radio set. This technology is adapted by the U.S. military for the production of anti-aircraft proximity fuses in World War II. The need for robust ordnance fosters the development of ceramic substrates and conductive inks.



April 6, 1938 Polytetrafluoroethylene (PTFE), a revolutionary new thermoplastic polymer, is discovered by Dr. Roy Plunkett at the DuPont Research Laboratories. First generation PCBs for microwave applications are a composite of PTFE and woven glass.

1950s G-10/FR-4 substrate material is introduced. A thermosetting industrial fiberglass composite laminate consisting of continuous filament glass cloth material with an epoxy resin binder has the characteristics of high strength, low moisture absorption, excellent electrical properties and chemical resistance.

1950s & 60s PCBs are common in consumer electronics; simple single-sided PCBs are the dominant variety and are still in use today.

1970s to present Multi-layer PCBs are widespread with advancements in isolation techniques and via technology. Since the 1980s, surface-mount construction replaces through-hole for cheaper assembly and smaller, more versatile multi-use circuits. Performance of polymer-based boards is tailored and enhanced, especially at higher frequencies, through the use of low profile ED copper conductors, low loss plating, various polymer chemistries and different fill materials (e.g., glass – random, woven, microsphere; ceramics and fibers).

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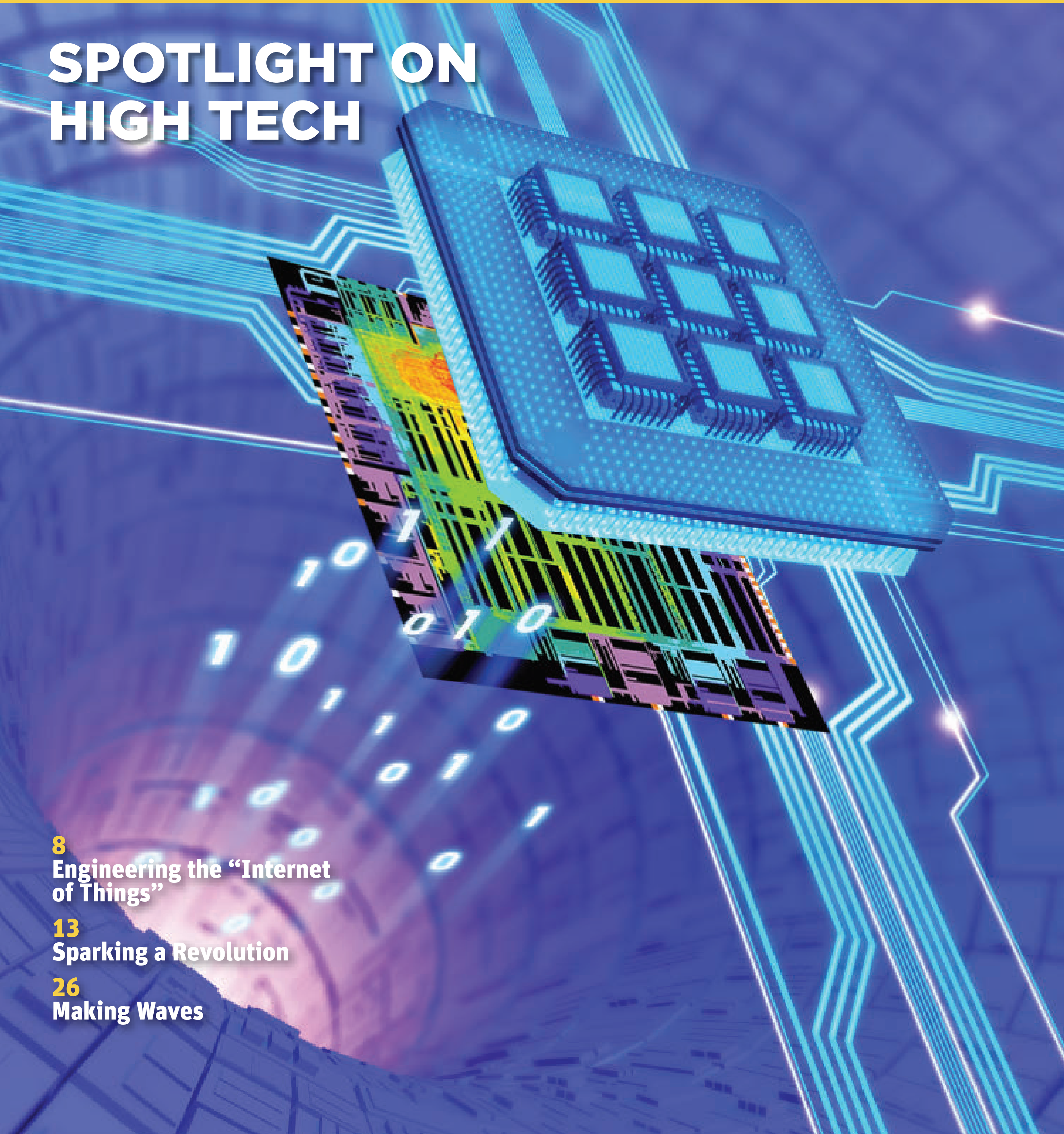

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Welcome to *ANSYS Advantage*! We hope you enjoy this issue containing articles by ANSYS customers, staff and partners. Want to be part of a future issue? The editorial team is interested in your ideas for an article. Contact us.

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DRIVING THE HIGH-TECH REVOLUTION

Fast-paced and hyper-competitive, the global high-tech industry is characterized by groundbreaking product innovations and rapid-fire market launches. Simulation provides an essential means for market leaders to quickly introduce revolutionary new features and functionality — while still honoring their foundational product promise.

By Sin Min Yap, Vice President Industry Strategy and Marketing, ANSYS

What's the hottest new high-tech product today? By the time this issue of *ANSYS Advantage* is published, that answer will have changed multiple times. Such is the nature of today's ultra-competitive global high-tech marketplace, in which every company seeks to introduce the next big innovation. More than ever, today's high-tech product development teams are pressured to quickly assess thousands of possible designs and identify the single, optimal solution that will have consumers marking the new product launch date on their calendars.

In their rush to innovate, high-tech companies cannot afford to make a single mistake. As they develop groundbreaking new products, they must actively seek out and address every potential cause of failure. In today's hyper-connected world, it doesn't take a product recall to ruin a brand's reputation. Even poor user reviews and ratings, shared via social media, can undo years of sound brand management. "Fail early and fail fast" is the new mantra, as engineering teams seek to eliminate faulty designs and potential weaknesses at the earliest possible development stage.

Given the combination of innovation, speed and quality demanded in this industry, it's no surprise that high-tech companies rely on simulation-driven product development. By designing and testing products in a risk-free, low-cost virtual environment, high-tech engineering teams can assess and discard dozens of ideas quickly, significantly compressing their design cycle. They can develop a complex product consisting of many systems, such as chip–package–board, in parallel, instead of optimizing one component at a time. They can consider multiple physics simultaneously, instead of conducting a series of single-physics studies.

In addition, engineering simulation helps high-tech product development teams manage design complexity, solving advanced problems such as reducing power consumption, delivering unwavering signal integrity, and improving bandwidth. With its multiphysics leadership, systems-level perspective and collaboration platform, ANSYS is uniquely qualified to help assess the many facets of high-tech product performance.

Engineering simulation will deliver game-changing product innovations.

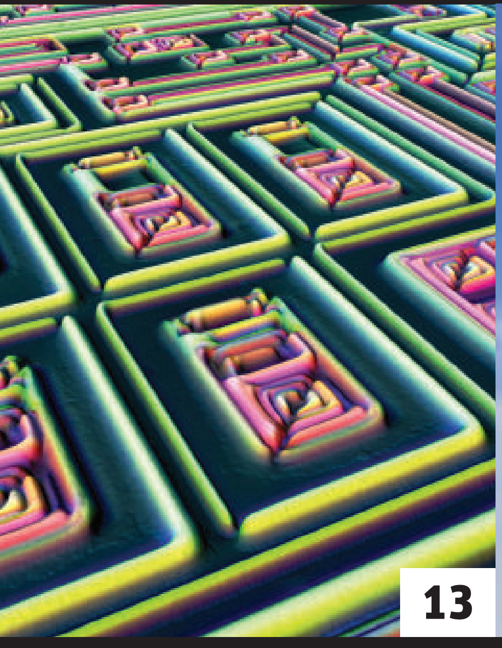
ROBUST ELECTRONICS
ansys.com/83hightech

Not only can ANSYS solutions identify obvious flaws, such as structural weakness in a tablet casing, but they can also flag the more subtle performance issues that are created when many disparate systems come together — for example, the effect of a variety of casing materials on thermal management, chip performance and electronic signal quality.

With a strong foundation in structural analysis, fluid dynamics and electronics, ANSYS provides high-fidelity simulation solutions that scale from integrated circuits, discrete components and embedded systems to fully functional products containing millions of lines of safety-critical embedded software.

While high-tech engineering teams face more pressures than ever, they also compete in one of the strongest and fastest-growing consumer markets today, creating incredible financial opportunities. According to industry analyst Gartner, in 2013 consumers bought 1.8 billion smartphones and 195 million tablet computers. Many of these devices were developed using ANSYS software.

As electronic devices continue to proliferate, engineering simulation will continue to help manufacturers not only make incremental improvements to key performance aspects such as speed and connectivity — but also deliver the game-changing product innovations that will have consumers lined up around the block.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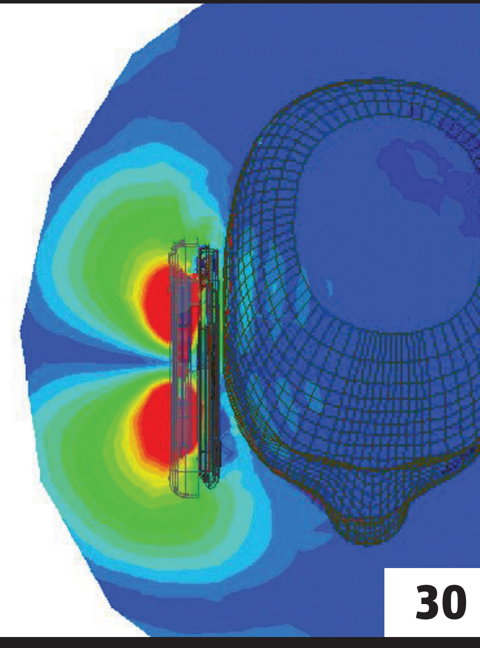
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WEB EXCLUSIVES
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ACADEMIC

Ice Breaker
Researchers have successfully tested a compact radar system integrated on a small lightweight unmanned aircraft system (UAS) to measure ice thickness and map underlying glaciers. The use of a UAS eliminates pilot risk and consumes only a fraction of the fuel necessary for a manned aircraft. ANSYS HFSS electromagnetic simulation software played a key role by helping to integrate the antennas onto the aircraft in much less time and at a much lower cost than would have been required with physical tests alone.

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The University of Pittsburgh and Carnegie Mellon University have teamed up with the Advanced Research Projects Agency–Energy and others to develop novel high-frequency, magnetic nanocomposite materials for power applications that can save materials and costs.

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Parsons Brinckerhoff used ANSYS Autodyn to perform three-dimensional coupled Euler–Lagrange (fluid–structure interaction) nonlinear finite element blast analysis to simulate explosions in a generic transit tunnel and predict the potential damage. Engineers were able to analyze the effectiveness of conventional protective measures, such as increasing the thickness of concrete lining or the amount of reinforcement steel, versus alternate protection measures to reduce damage to the lining and determine costs.

ABOUT THE COVER

High-tech market leaders rely on simulation-driven product development to launch their devices quickly, cost-effectively and with a high degree of confidence that they will perform as expected in the real world.

Simulation in the News

VIRTUAL HEART: HOW ENGINEERING IS HELPING MEDICINE

BBC News
bbc.com, May 2014

Sheffield University is a leading center for in silico medicine and intends to map the entire human body with software. Models assist medical professionals in diagnosis, treatment and even clinical trials. For example, although doctors can identify coronary artery disease by viewing a series of X-rays, simulation can deliver vital information such as blood pressure and flow changes.

WHEN A DRONE FLIES INTO A JET ENGINE, BAD THINGS HAPPEN

Defense One
defenseone.com, May 2014

The sky is crowded with airplanes, drones and animals, as evidenced by recent multiple near-collisions. As more drones take to the skies, pilots and engineers are increasingly concerned that a drone flying too close to an airplane might be sucked into the engine. Robert Harwood of ANSYS states that a drone strike would be much like a bird strike, but could cause significantly more damage to the engine. Engine regulations help to ensure that damage is localized if the engine blades break in the event of a collision.

ANSYS ENSURES STRUCTURAL INTEGRITY OF 2014 FIFA WORLD CUP STADIUM

CIOL
ciol.com, June 2014

Football fans attending the FIFA World Cup games in Brazil were able to cheer on their teams and focus on the action without being concerned about any structural issues. Specialists at ANSYS channel partner ESSS and the University of São Paulo analyzed the Estádio Nacional Mané Garrincha stadium with ANSYS multiphysics software to predict airflow around the stadium and pressures on the stadium roof to account for the combined effects of wind, stadium infrastructure and a traditionally rowdy crowd. Engineers suggested several changes to improve the integrity of the stadium and the safety of both players and fans based on the results of the simulations.

▲ Simulation of tension in the metallic structure of cables and trusses for a World Cup stadium

EPA SELECTS ANSYS FOR SIMULATION SOFTWARE TO DEVELOP ADVANCED TEST ENGINE

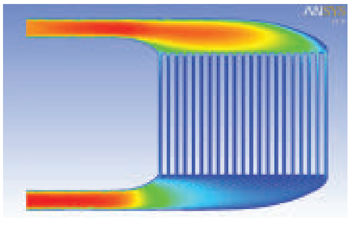
Green Car Congress
greencarcongress.com, July 2014

Development of a new fuel-saving and emissions-reducing test engine is under development by the U.S. Environmental Protection Agency (EPA) with the help of ANSYS simulation software. The goal is to produce an engine that will help meet recently issued fuel standards through improvements to combustion chamber geometries, fuel injection strategies, fuel composition, valve timing and intake conditions. With ANSYS FORTÉ, the EPA can reduce the need for expensive and lengthy physical prototyping in favor of engine design in a virtual setting to reduce both cost and time between design iterations.

ANSYS DRIVES ELECTRIC VEHICLE INNOVATION WITH GM, NREL AND ESIM

Bloomberg Businessweek
businessweek.com, June 2014

The world is closer to realizing affordable and eco-friendly electric vehicles. A project to design better, safer and longer-lasting lithium-ion EV batteries using ANSYS software is contributing to this goal. ANSYS, General Motors, the U.S. Energy Department's National Renewable Energy Laboratory and ESim are working to produce models to improve battery design with optimized performance, safety and lifespan, all within shorter design cycles.

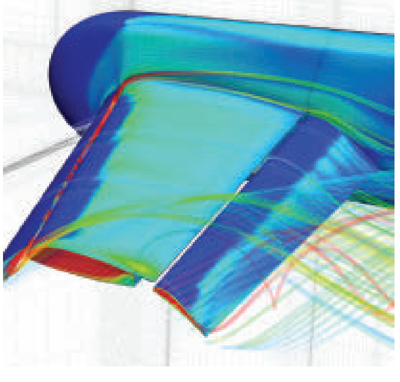


▲ 20-cell battery model

MODELING AND SIMULATION LIFT AEROSPACE CONTROL SYSTEMS

E&T Magazine
eandt.theiet.org, July 2014

Diversity in the aerospace industry is rapidly increasing, including everything from helicopters to airplanes to drones. Design requirements for different structures and materials drive engineers to rapidly model and simulate the aerodynamic performance of the airframe and evaluate the materials used in construction. Simulation is also used in the design of flight control systems that integrate the structure and control components. These components include most — if not all — of the electronics used on an airplane, from the aircraft's aileron and other control surfaces to the black box flight recorder. Engineers employ ANSYS software to ensure structural integrity as well as to find electromagnetic solutions to enhance safety and comfort for passengers and crew.



▲ Aeroelastic wing simulation example

YC-BACKED RIGETTI COMPUTING RAISES $2.5M TO CREATE COMMERCIAL QUANTUM SYSTEMS

TechCrunch
techcrunch.com, August 2014

Many companies are attempting to incorporate quantum computing into commercial hardware. Rigetti Computing wants to be a leader in this effort, providing consistent performance improvements through an ANSYS-powered prototyping process. The major issues with quantum computing include unpredictable performance and high costs. ANSYS solutions help Rigetti rapidly test changes without having to build new circuitry with each iteration. This advancement could allow computers to perform certain kinds of operations immeasurably faster than traditional processors.

RAISING THE ABSTRACTION OF POWER: TRENDS

Semiconductor Engineering
semiengineering.com, July 2014

Design requirements for today's system-on-chip (SoC) devices need a comprehensive power analysis methodology from system to register-transfer-language (RTL) to gate for successful system design for power management. System designers historically used complex spreadsheets to calculate power consumption, which led to problems like limited reuse, cumbersome sharing, error-prone formulas and no dynamic system results. A reliable alternative is performing simulation at many points in the design to achieve systems-level power savings.

4MOMS LEVERAGES ANSYS TO DEVELOP INNOVATIVE PRODUCTS

Wall Street Journal
wsj.com, July 2014

4moms is revolutionizing the $8.9 billion baby gear market with some help from ANSYS. Engineering simulation tools allow engineers at 4moms to create virtual prototypes to reduce time and money, while maintaining product quality. Using simulation from ANSYS, 4moms engineers validated certain design decisions before crash testing and supplemented the crash-testing results, enabling the company to operate more effectively and efficiently.

ORIGAMI UNFOLDS A NEW WORLD OF SHAPE-SHIFTING ELECTRONICS

CNET
cnet.com, May 2014

Electrical engineering is taking a large step forward using the mathematical properties of origami. Electronic devices that compress and change shape are possible if designed correctly. Companies could put tiny devices into compact spaces by morphing forms to optimize space usage. A leading electromagnetics specialist and his team from Florida International University and Georgia Tech University are leading the development of origami-influenced antennas. ANSYS HFSS allows the team to conceptualize new antenna models with only one limit: imagination. The software permits designers to work through many different designs without expensive physical prototyping.

ENGINEERING THE "INTERNET OF THINGS"

Our world is more connected than ever, thanks to the growing web of visible and unseen electronics that surround us every day. ANSYS provides the comprehensive suite of simulation software to reliably and cost-effectively engineer high-performance electronic devices and systems.

By Sudhir Sharma, Director of High-Tech Industry Strategy and Marketing, ANSYS

Consumers' expectations for connectivity, energy efficiency, reliability, light weight and structural strength will only increase.

Today we live in a world based on connectivity and communication, in which a burgeoning network of electronic systems and devices helps us navigate our days.

Smartphones, tablets and GPS systems are the most obvious examples, but consider the increasingly sophisticated electronics in cars, homes, hotels and offices that keep us secure and comfortable, or the medical implants and prosthetics on which many people rely for everyday health. When we visit theme parks or attend concerts, we are likely to scan a wristband or smartphone for admittance. Wearable wristbands and activity trackers can monitor our physical movements, vital signs and sleep patterns. Today, high-tech devices are inescapable.

The high-tech industry has coined the term "Internet of Things" (IoT) to describe this proliferation of electronic devices and systems. There can be no doubt that the Internet of Things is poised to change the way we live, work, interact and seek out entertainment. As consumers, we can look forward to many conveniences; for businesses, the IoT represents an incredible opportunity to revolutionize the product development value chain. While 2 billion smart devices were sold in 2006, it's estimated that this figure will grow to 200 billion by 2020. Devices will outnumber people by a ratio of 26 to one. [1]

WEARING A WIRE
ansys.com/83IOT1

DESIGNING RF ANTENNAS FOR WEARABLE ELECTRONICS AND THE INTERNET OF THINGS
ansys.com/83IOT2

BIG GROWTH, BIG CHALLENGES

This rapid growth brings significant challenges. As devices proliferate, consumers' expectations for connectivity, energy efficiency, reliability, ease of use and structural strength will only increase. Electronics must be not only innovative and high-performing, but also attractive. And, of course, all this functionality and beauty must be delivered at a low price.

How can high-tech engineering teams manage these pressures? Since the industry's inception, market leaders have relied on simulation-driven product development to launch their devices quickly, cost-effectively and with a high degree of confidence that they will perform as expected in the real world.

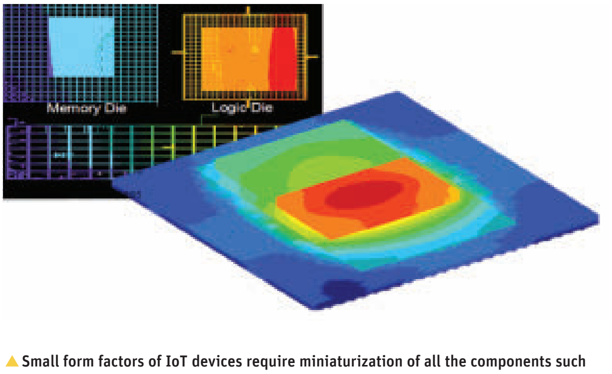
For high-tech manufacturers, engineering simulation is the key. Designing products in a risk-free, low-cost virtual space enables engineers to quickly consider thousands of designs, without investing time and money in physical prototypes. They can choose a few promising designs, then subject them to thousands of operating parameters — again, with no investment in physical testing. Engineers can perfect product components or optimize entire systems. They can consider one physics area or the complete range of forces that will be brought to bear on their designs.

ANSYS: A HIGH-TECH RESOURCE FOR HIGH-TECH TEAMS

When we talked to industry expert Ed Godshalk at Maxim Integrated — a world leader in analog semiconductors — he said, "When you consider the complexity of designing and packaging an electronic system, it's really impressive that ANSYS software can support that full development cycle." (Read more insights from Godshalk in the feature on page 13.)

That range of capabilities is the result of focused software development investments, as well as strategic acquisitions, that have positioned ANSYS to support the complete design cycle for high-tech devices, including integrated circuits (ICs) and embedded software. Throughout this issue of *ANSYS Advantage*, you'll see how customers are leveraging ANSYS software every day, and at every stage of the development cycle.

Recently, ANSYS has developed comprehensive solutions for both robust electronic systems design and advanced material systems design for high-tech engineers. These solutions address key challenges for high-tech designers: improving speed and bandwidth, maximizing power and energy efficiency, optimizing antenna performance, and incorporating advanced materials. The sections that follow provide greater insight into these challenges as well as relevant ANSYS solutions.



▲ Small form factors of IoT devices require miniaturization of all the components such as 3D ICs. ANSYS IC tools help validate power noise and reliability of stacked-die chips using the latest silicon process technology.

Functionality and beauty must be delivered at a low price.

High-tech-industry product development teams routinely use coupled multiphysics software from ANSYS to analyze the trade-offs among speed, bandwidth, signal integrity, power integrity, thermal performance and EMI/EMC.

RAMPING UP SPEED AND BANDWIDTH

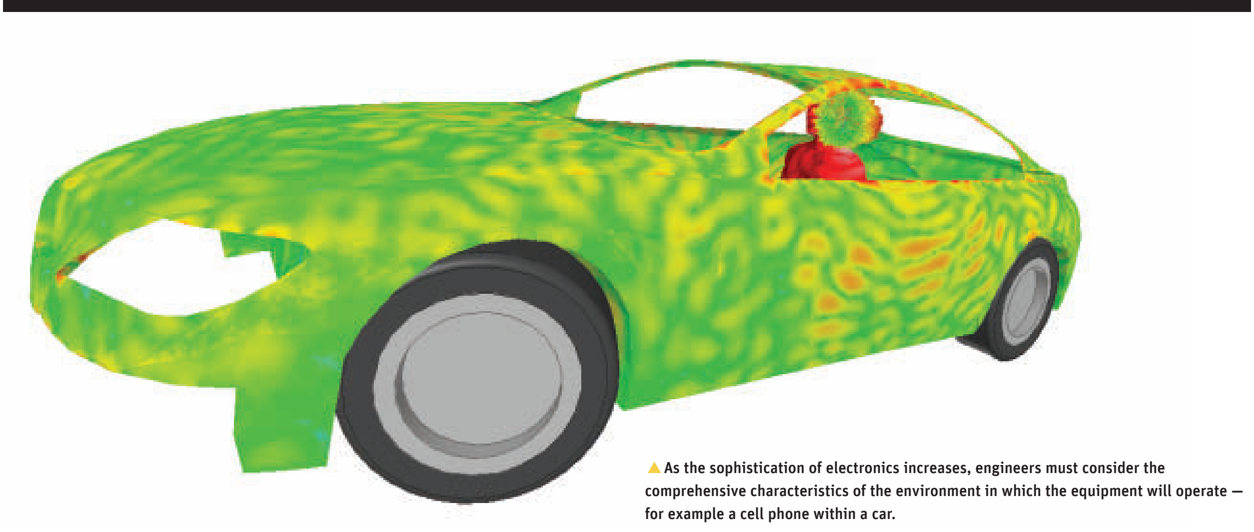
As mobile devices proliferate, more and more data is being transmitted and received, driving the need for faster wired and wireless communications networks. Video streaming, interactive gaming and high-speed web service are pushing the limits of not only mobile devices, but also servers, routers and switches. Improving speed and bandwidth is an industry imperative, but design complexity poses a significant challenge.

For example, designing printed circuit boards (PCBs) for high-speed, double data rate memory buses or serial communication channels requires extreme care. High data rates combined with low operating voltages can cause signal and power loss. In today's device-crowded world, electromagnetic interference (EMI) and electromagnetic compatibility (EMC) issues also affect power integrity (PI) and signal integrity (SI).

The ANSYS Nexxim circuit simulator (part of the ANSYS HFSS SI option and ANSYS SIwave) offers an efficient way to design and test memory channels for servers that power our cloud-computing world. When this simulator is used in combination with IBIS-AMI, or Nexxim's QuickEye and VerifEye models, it represents the industry's leading solution for high-speed communication channel design.

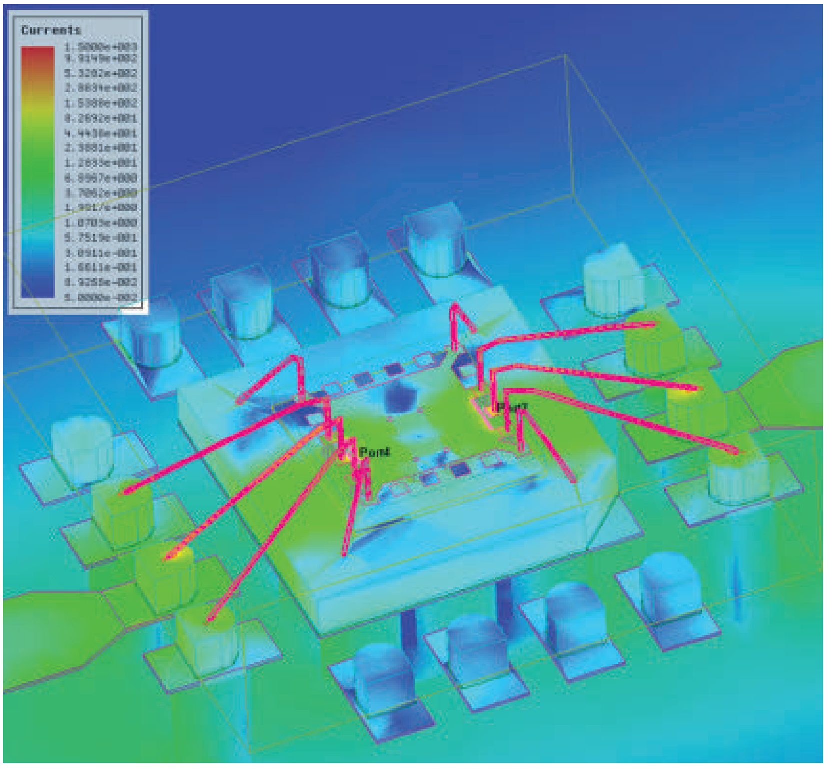
End-to-end design and optimization for complex high-speed electronic devices is faster, easier and more accurate thanks to new functionality in the ANSYS SIwave electromagnetic simulation suite for the design of high-speed PCB and IC packages. This functionality is available via three targeted products: SIwave-DC, SIwave-PI and SIwave. Engineers can quickly identify potential power and signal integrity problems with increased flexibility, and more easily access a complete set of analysis capabilities that they can leverage throughout the design cycle.

High-tech–industry product development teams routinely use coupled multiphysics software from ANSYS to analyze the trade-offs among speed, bandwidth, signal integrity, power integrity, thermal performance and EMI/EMC. For example, a smartphone manufacturer recently leveraged a suite of ANSYS software — including ANSYS HFSS, ANSYS Icepak, ANSYS Mechanical and ANSYS



As the sophistication of electronics increases, engineers must consider the comprehensive characteristics of the environment in which the equipment will operate — for example a cell phone within a car.

ANSYS software provides critical capabilities in multiphysics, systems-level simulation that will drive the continuing growth of the IoT.



Designing printed circuit boards (PCBs) for high-speed, double data rate memory buses or serial communication channels requires extreme care. High data rates, combined with low operating voltages, can cause signal and power loss. Simulation of current distribution in a package is shown.

DesignXplorer — to significantly accelerate the development of a smartphone shielding system to maximize data speed and throughput.

At Alcatel-Lucent, engineers are using ANSYS HFSS to ensure integrity and reliability, while also minimizing costs, as they link ICs on two separate boards across a high-speed channel. (See story on page 37.)

OPTIMIZING POWER AND EFFICIENCY

Few issues are as important in the high-tech industry as effective power management. To help address this issue, ANSYS has created a strategic initiative centered on supporting the design of robust, power-efficient electronics.

Traditionally, engineers analyzed power consumption and delivery issues via a siloed approach, looking separately at the chip, board and package. Today, ANSYS supports the industry's only truly integrated chip–package–system (CPS) design methodology, which allows component optimization — as well as co-analysis and co-optimization across the entire system. This approach balances the lower operating voltages needed to conserve power with the consistency and reliability required to eliminate field failures.

By combining advanced physics solvers with industry-leading solutions for power-efficient electronics design, engineers can confidently predict systems-level performance at an early design stage, long before lab system integration. The resulting capabilities for full electromagnetic extraction, SI/PI/EMI analysis, chip-level power optimization and reliability verification, and thermal and mechanical stress simulation are unmatched in the high-tech industry.

ANSYS also fosters partnerships with high-tech industry leaders to create unique simulation capabilities. For example, ANSYS and Intel® Custom Foundry teams have developed reference flows using ANSYS RedHawk for system-on-chip (SoC) power and electromigration sign-off, ANSYS Totem for custom intellectual property (IP) power — and EM — integrity, and ANSYS PathFinder for full-chip electrostatic discharge validation.

This collaboration extends the work on the Intel Custom Foundry 22 nm process design platform to the 14 nm platform. The 14 nm Tri-Grate process technology enables chips to operate at lower voltages with lower leakage, providing chip designers with the flexibility to choose transistors targeted for low power or high performance, depending on the application.

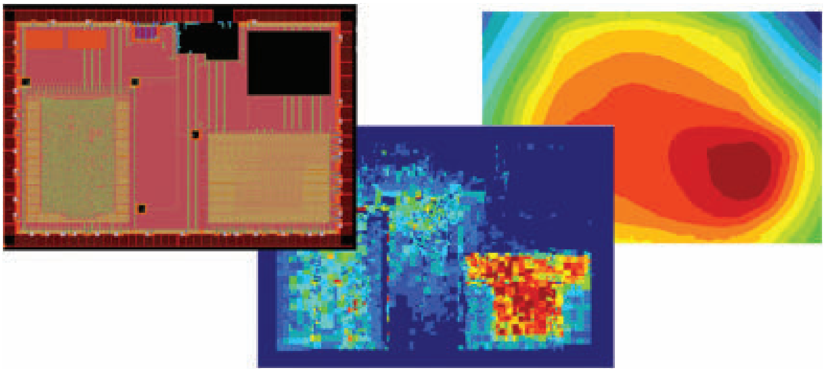
ANSYS is continually developing newer and better methods to ensure design robustness at the earliest possible stage.

INTEGRATED CHIP-PACKAGE-SYSTEM SIMULATION: THE COMPLETE ELECTRONICS SOLUTION FROM ANSYS AND APACHE
ansys.com/83IOT5

STAYING CONNECTED

The proliferation of wireless devices creates new performance demands for antennas and radio systems, which need to deliver uninterrupted connectivity.

In designing antenna systems, engineers must consider the comprehensive characteristics of the environment in which the antenna will operate. This can include modeling such effects as a plastic covering over the antenna, the interaction of a mobile handset with the human hand, or the way an antenna is installed in an automobile. With so much functionality crowded into devices — and so many wireless systems residing in close proximity — EMI is on the rise.



▲ Every electronic device contains one or more integrated circuits that need to deliver power, performance and reliability. ANSYS IC tools provide comprehensive analysis coverage, including power integrity, electromigration and thermal reliability within the context of the entire system.

Engineers are also challenged to develop new antenna technologies that require multiple frequency bands and greater efficiency, all within a smaller physical profile.

ANSYS is the industry leader in simulating the performance of antenna, microwave, wireless and radio frequency (RF) systems. With new solver capabilities in ANSYS HFSS — such as finite element method (FEM) domain decomposition, 3-D method of moment (MoM) and hybrid FEM–MoM — antenna engineers can rapidly solve electrically large, full-wave electromagnetic models. These models can accommodate regions of complex materials, as well as geometries with outer regions that are electrically large. In addition, transient solutions allow engineers to examine the behavior and scattering of radiation across time and space.

While antenna models are very large, high-performance computing (HPC) capabilities from ANSYS allow engineers to increase problem size and complexity while minimizing time-to-solution. Engineers at Synapse — a leader in wearable electronics — have used ANSYS HFSS in an HPC environment to increase antenna range by a factor of five, while reducing their overall design cycle by 25 percent.

At Vortis, engineers are applying ANSYS software to solve the problem of wasted RF energy in cell phones, which not only reduces battery life but also creates acoustic noise. The company's innovative new phased-array antenna system is just one example of how simulation-driven product development is impacting the future of the IoT. (See page 30.)

INCORPORATING ADVANCED MATERIALS

At ANSYS, today there is a cross-industry strategic initiative aimed at supporting the incorporation of advanced composite materials into the product development process — and with good reason. Composite materials are no longer used only by automakers and aerospace manufacturers.

Today, high-tech companies turn to advanced lightweight, yet strong, materials to create flexible mobile and wearable electronics. However, a range of complex issues must be considered when evaluating new materials — including electrical conduction properties, structural strength, dimensional stability over time and resistance to thermal build-up. Design for manufacturability is also an important consideration.

High-tech engineers simulate the assembly of composite layers and conduct finite element analysis via ANSYS Composite PrepPost and other specialized modeling tools, subjecting these models to a range of real-world conditions. Electrical performance is verified using ANSYS HFSS and ANSYS SIwave, while ANSYS Icepak analyzes the thermal performance of electronic systems and devices.

ANSYS offers the industry's most comprehensive solution for evaluating the potential of advanced materials to reduce weight, while also optimizing conductivity, signal integrity, dimensional stability and thermal management within devices. For example, 3M recently published a groundbreaking study on how a novel embedded-capacitance composite material affected the electrical performance of a printed circuit board, relying on ANSYS SIwave to model the new board versus a conventional PCB. [2]

At the University of Pittsburgh and Carnegie Mellon University, engineers are using ANSYS PExprt and ANSYS RMxprt to assess the performance of new nanocomposites that have the potential to revolutionize power transformer technology. (Learn more in our Web Exclusive.)

INVESTING IN THE FUTURE

Since the earliest days of the high-tech revolution, simulation-driven product development has been a critical strategy for satisfying consumers' increasing demand for device functionality, speed, bandwidth, aesthetics and other product characteristics — while still meeting revenue and margin goals. ANSYS has helped hundreds of high-tech companies launch their game-changing designs quickly, cost-effectively and confidently, creating market leadership and building some of the industry's strongest brand reputations.

Historical trends enable us to confidently predict that high-tech manufacturers will continue to deliver incredibly innovative products that we cannot even imagine today. We can also be confident that — with a commitment to strategic acquisitions as well as development of new software features and functionality — ANSYS will continue to invest in our high-tech customers' success.

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intel.com/content/www/us/en/internet-of-things/infographics/guide-to-iot.html

[2] Simulation and Design of Printed Circuit Boards Utilizing Novel Embedded Capacitance Material

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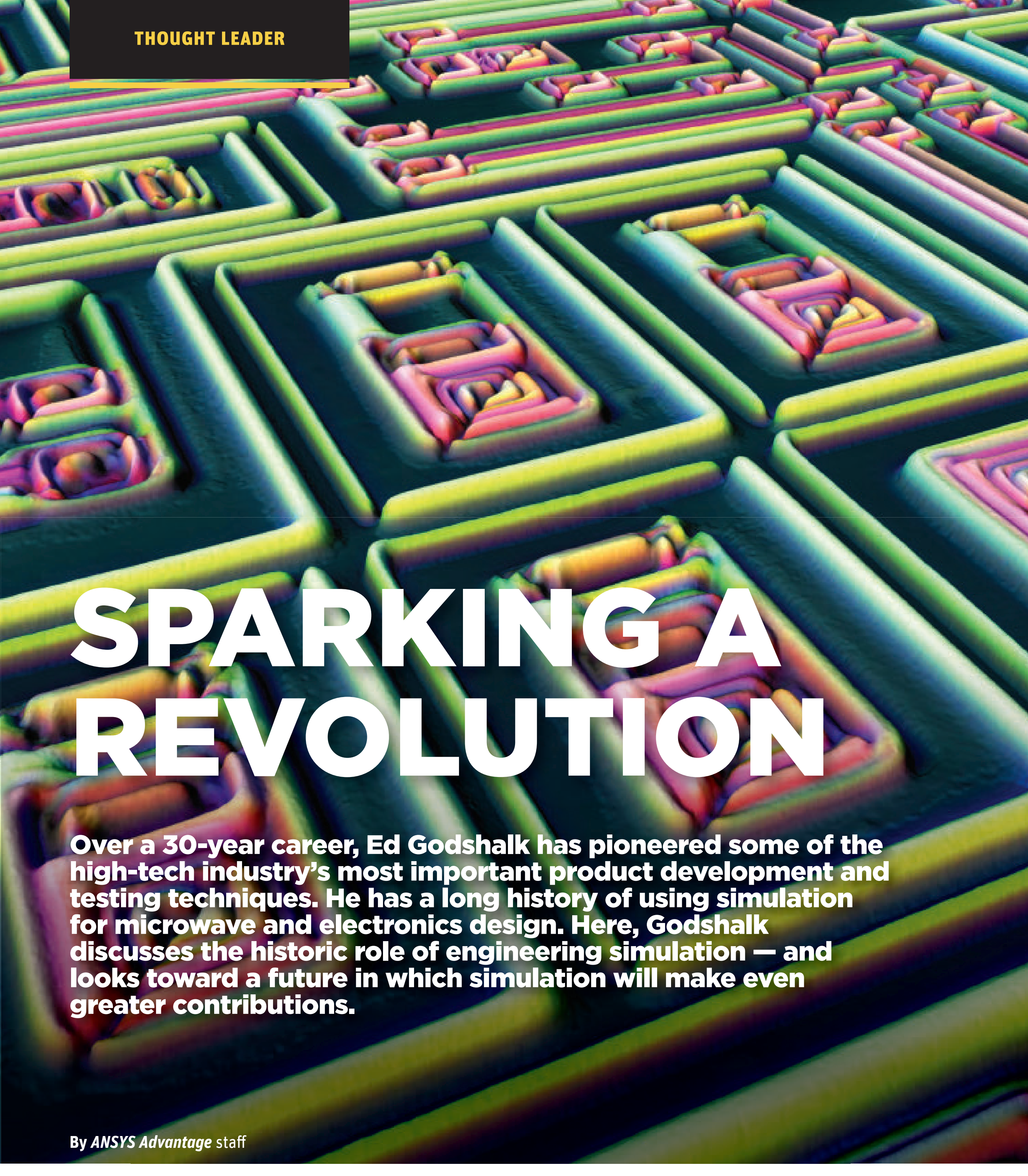
THE RACE TO 6G — FASTER NETWORKS AND DEVICES PROMISE A WORLD OF NEW POSSIBILITIES
ansys.com/83IOT3

HIGH-PERFORMANCE ELECTRONIC DESIGN — PREDICTING ELECTROMAGNETIC INTERFERENCE
ansys.com/83IOT4



SPARKING A REVOLUTION

Over a 30-year career, Ed Godshalk has pioneered some of the high-tech industry's most important product development and testing techniques. He has a long history of using simulation for microwave and electronics design. Here, Godshalk discusses the historic role of engineering simulation — and looks toward a future in which simulation will make even greater contributions.

By *ANSYS Advantage* staff

Since his career began in the early 1980s, Ed Godshalk has always had a dual focus: designing higher-performing electronics components and systems, while also developing the underlying test and measurement tools and processes that enable true product innovation. He has pioneered a number of measurement methods and systems for product development that have helped shape the modern high-tech industry. For example, while at Cascade Microtech in 1990, Godshalk designed the world's first waveguide input wafer probe, which covered V-band (50 GHz to 75 GHz), and later W-band (75 GHz to 110 GHz). This enabled development of early millimeter-wave integrated circuits.

Today, Godshalk is a distinguished member of the technical staff and director of the Electromagnetics Group at Maxim Integrated, one of the largest analog semiconductor manufacturers in the world. He manages an expert staff charged with developing advanced models and measurements necessary for Maxim to introduce advanced products.

Engineering simulation created the foundation for the incredible gains we have realized in electronics performance and the impressive degree of innovation we have witnessed in the high-tech industry.

These products are used by leaders in mobility and consumer products such as Samsung; major automakers in Asia, North America and Europe; medical device manufacturers; and large search engine and social media companies.

Recently, Godshalk shared his perspective on simulation, as well as his view from the front lines of the high-tech industry's ongoing battle to combine high product quality with low cost and speed to market. While virtual product development practices first revolutionized the high-tech industry 30 years ago, Godshalk believes that the future holds even greater potential for high-tech engineering teams to leverage value from simulation-driven product development.

SYSTEMS ENGINEERING FOR SMART PRODUCTS
ansys.com/83sparking1

You have a long history of using simulation in the high-tech industry. How did it change your work as an electrical engineer?

It's impossible to overstate the value that engineering simulation brought to the table 30 years ago. In the early 1980s, the standard way to design microwave circuits was via graphs, equations and a lot of complex math. This was the situation when I was a student and young engineer. Often the only way to test those systems was to physically construct large-scale physical models, which were expensive, unwieldy and heavy. One example, made in aluminum, weighed more than 300 pounds! When I began using microwave circuit simulation in the mid-1980s and HFSS 1.0 to simulate full-wave electromagnetic fields in the 1990s, it was a true game-changer. Suddenly, there was software that could not only automate and accelerate all the complicated math involved in systems design, but also support rapid virtual prototyping and testing. Simulation software was such a powerful tool that it increased the productivity of development staff involved in electromagnetic simulation problems by something like 10 times. Engineering simulation really created the foundation for the incredible gains we have realized in electronics performance. It laid the groundwork for the impressive degree of innovation we have witnessed in the high-tech industry. Simulation removed the obstacles to fast, confident, cost-effective product innovation. It eliminated the time and money wasted on tedious, trial-and-error circuit testing. It changed everything.

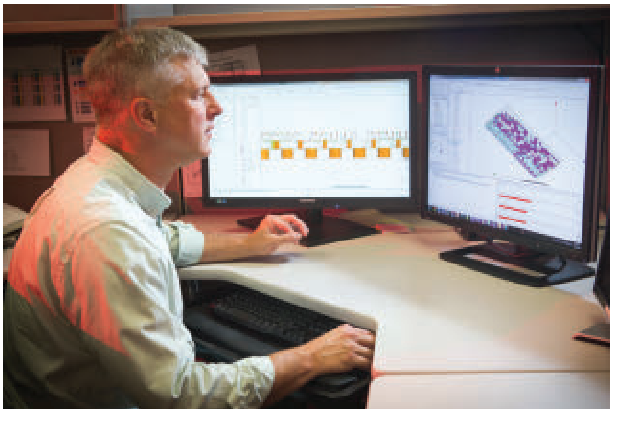
ANSYS helps with understanding and solving today's advanced development challenges.

How does engineering simulation add value for your team at Maxim Integrated today?

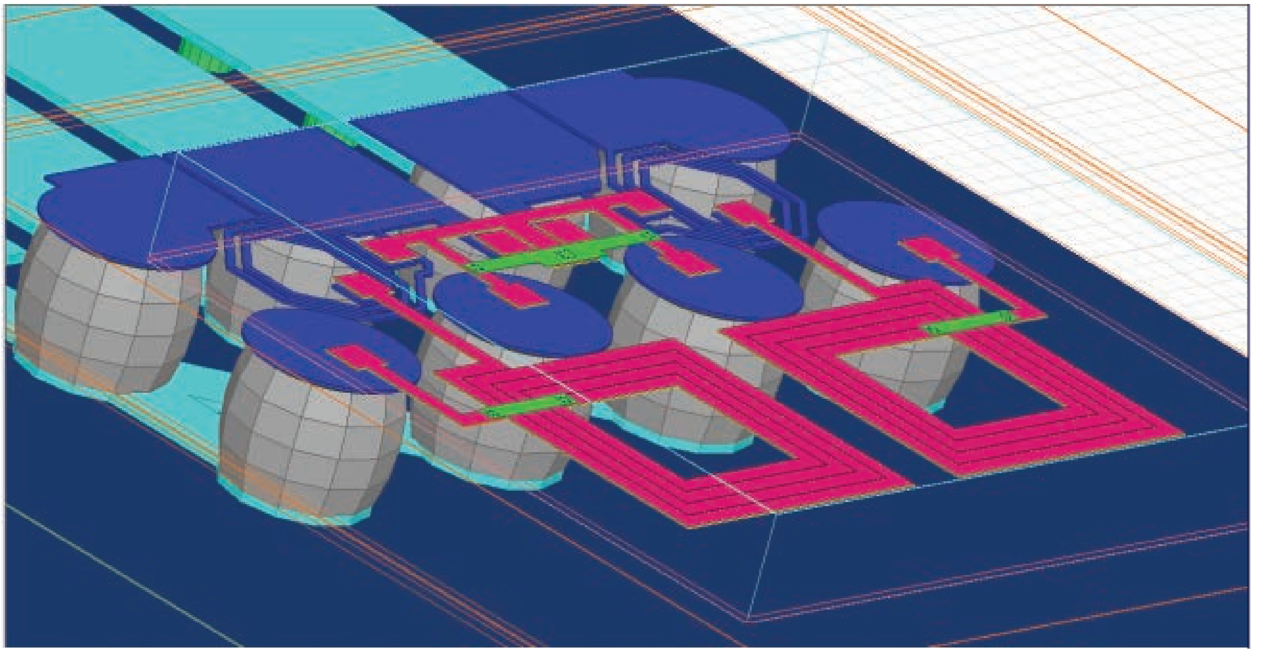
There is strong consumer demand for increased functionality of electronic devices and connectivity. At Maxim, we help our customers offload some of their engineering costs by reducing part counts. That means placing more and more functionality into each of our systems, while maintaining or even reducing their physical profile and cost. But this raises complex issues. How will signal integrity be affected when functions reside so close together? Will thermal build-up be a problem? A suite of ANSYS software — including HFSS, SIwave, Maxwell and Q3D Extractor — helps to understand the trade-offs and maximize system performance. Today, engineering simulation is an even more vital capability than it was 30 years ago. ANSYS helps with understanding and solving today's advanced development challenges.

What changes have you seen in simulation software and practices over the years?

As our design challenges have become more complex, fortunately both software and hardware have evolved to help meet these new challenges. In terms of software, ANSYS solutions



Engineers at Maxim Integrated must place more and more functionality into each system, while maintaining or even reducing their physical profile and cost. The company uses the suite of ANSYS electronics software to understand the trade-offs and maximize system performance.



S-parameter model for IC die in package on PCB

are much more integrated today, making it easier to bring multiple tools to bear on a single design problem. ANSYS software is also more comprehensive. When you consider the complexity of designing and packaging an electronic system, it's really impressive that ANSYS software can support that full development cycle.

In the area of best practices, a great impact resulted from the introduction of high-performance computing (HPC) resources — and the simultaneous launch of simulation software that's customized for HPC environments. At Maxim, we're focused on high-complexity, numerically large design projects. ANSYS HPC Packs and multi-core processors help improve time to market. We run quite a few eight-core processors and even a 32-core processor. Engineering simulation has enabled the development of faster computers, which in turn have enabled larger, faster simulations. It's really a closed-loop process that keeps making our electronics simulation capabilities better and better.

PRODUCT INTEGRITY IN A NEW WORLD OF SMART PRODUCTS
ansys.com/83sparking2

You mentioned cost control as a priority for your customers. What other challenges do they face?

Some of the biggest challenges in the high-tech industry center on power — harvesting it, converting it, storing it and using it more effectively. To make futuristic product ideas — like wearable electronics — practical, the development of radically new power technologies that maximize efficiency, while minimizing impacts on the environment, will be important.

Product miniaturization is also a huge focus for our customers because consumers want their phones, tablets and other technologies to be as small as possible without losing any functionality. Our customers also are trying to increase data transfer speed and bandwidth — again, to meet consumer needs for uninterrupted content. Connectivity and signal integrity are related consumer concerns that our customers focus on.

While these are daunting challenges, the good news is that ANSYS software and simulation-driven product development can help us overcome them. Simulation allows us to study all these problems in depth and arrive at optimized solutions.

How would you describe your relationship with ANSYS over the past three decades?

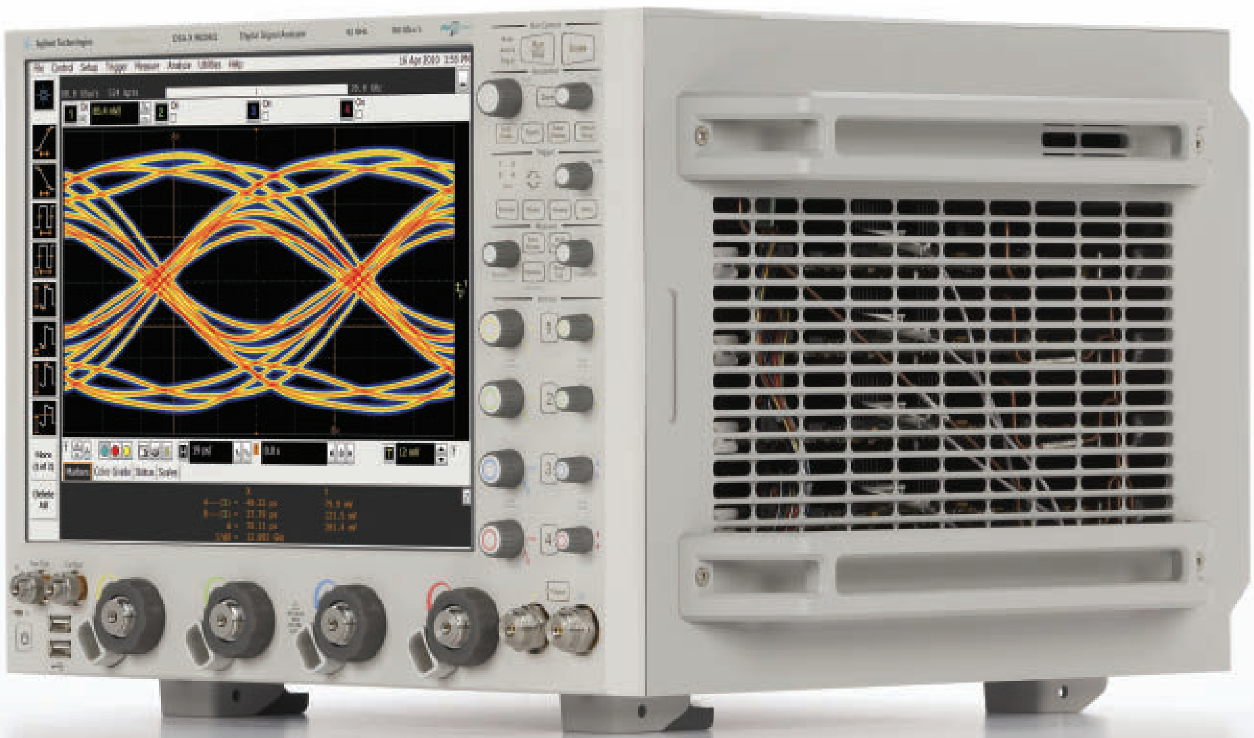
I was an early customer of Ansoft (the company that developed HFSS and is now part of ANSYS), and today Maxim Integrated leverages a wide range of ANSYS solutions. I think that gives me a unique perspective. ANSYS solutions have always been very intuitive and easy to use, and the graphical user interface just keeps improving. It's very easy for new users to get up and running. The company also has great customer support. My team and I have had a strong, collaborative relationship with both ANSYS customer service staff and software developers over the years.

I have observed that ANSYS has done a great job at keeping up with trends in the high-tech industry. When we needed to model larger systems or work in an HPC environment, ANSYS had the software tools ready. As the job of electrical engineers has evolved, the software company has been right there with us in terms of technology development.

In the future, our industry is going to produce all kinds of high-tech electronic innovations. I firmly believe that ANSYS software will significantly contribute to their development.

HOT BOX

Simulation helps cool the calibration head for the world's fastest real-time oscilloscope.

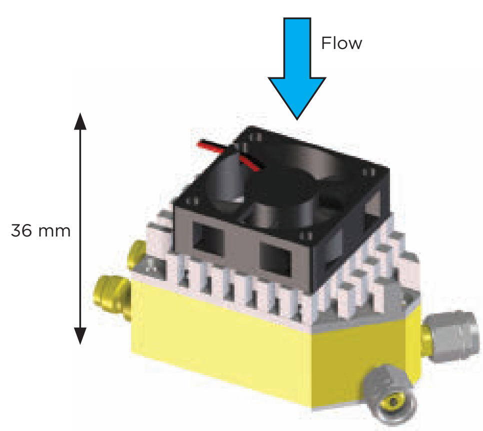


By Matt Richter, Expert R&D Engineer, Keysight Technologies, Santa Rosa, U.S.A.

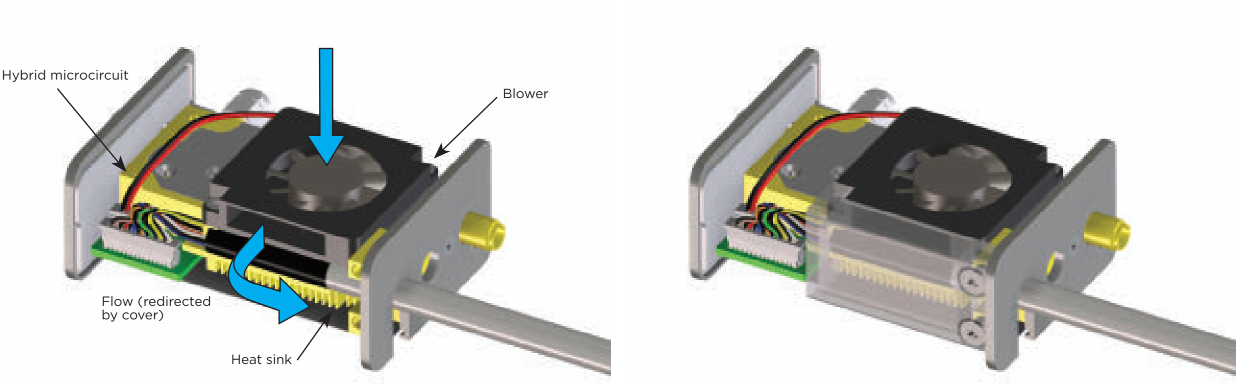
Oscilloscopes are digital instruments that display and measure the wave shape of an electrical signal. High-performance oscilloscopes, which are capable of measuring signals at very high frequencies, are used primarily in high-speed serial communications, radio frequency/radar/aerospace and high-speed physics applications.

Keysight Technologies (formerly Agilent Technologies), which bills itself as the world's premier test and measurement company, develops equipment with breakthrough capabilities that help solve tough measurement challenges. For example, the Infiniium 90000 Q-Series oscilloscope is the first to reach the 60 GHz barrier, enabling engineers to make measurements on a new generation of fiber-optic transponders and systems that provide higher levels of data communications speeds than previously possible.

As part of the design of the world's highest-bandwidth real-time oscilloscope, Keysight Technologies determined that it needed to develop a new electrical calibration source to ensure



▲ Typical fan/heat exchanger configuration



▲ Final head design using cross flow. Image on left is without a cover; image on right shows transparent cover.

that the oscilloscope could set a new standard for measurement accuracy. This design of the calibration source (Agilent N2806A) involved challenging electrical, mechanical and thermal requirements. Keysight utilized ANSYS CFX computational fluid dynamics (CFD) software to model the environment and produce a design that could exceed all of the requirements. Keysight delivered a first-pass success on the design and is now shipping the world's highest-bandwidth real-time oscilloscope based on this calibration technology.

The major challenge in designing the package for the calibration head was cooling. The head contains two integrated circuits (ICs) that dissipate a total of 3.2 watts within a 35-mm-wide by 42-mm-long by 15-mm-high box with 5,250 mm^2 surface area. Because of the limited size of this box, the energy released by the circuits produces a considerable temperature increase, which can adversely affect handling comfort. The packaging is built around a machined-aluminum base incorporating the heat sink and cavities for mounting the ICs. To address this cooling challenge, the engineers decided to try a cross-flow heat exchanger approach even though they had no experience with this configuration. Building physical prototypes would normally take up to eight weeks and require first-pass success with the prototypes to ensure on-time project completion. Instead, Keysight engineers turned to ANSYS CFX computational fluid dynamics (CFD) software to model and simulate the cross-flow configuration. They first performed an airflow-only analysis to determine pressure drop, then followed up with a heat-transfer analysis to determine temperature rise. The design created with the aid of simulation worked perfectly when production parts were built.

EVALUATING ALTERNATIVE COOLING DESIGNS

Before employing simulation, Keysight engineers made a quick calculation to determine if the unit could be cooled with free convection using a formula to determine temperature rise in a package. In this case, the rise was predicted to be 86 C, much higher than the design specification of 15 C — the limit at which the device can be comfortably handled. Forced air was needed to cool the head, but what type of forced-air cooling would provide the best results? The fan/exchanger configuration that Keysight normally uses positions the fan on top of the head blowing air downward onto the heat sink and exiting around the sides of the unit. This approach requires a relatively large package height, and the connectors need to be positioned toward the edge of the unit, which was not compatible with the connector placement on the front of the instrument that the head was used to calibrate.

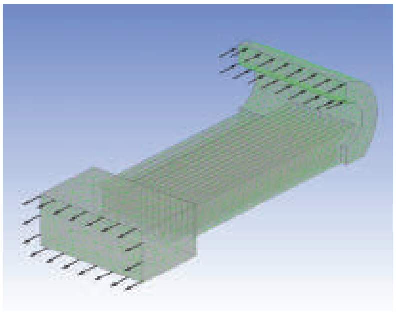
Keysight engineers then looked at the alternative of a blower/cross-flow heat exchanger design in which the airflow is perpendicular to the face of the heat sink. In this application, the inner walls of the case form a curved channel that directs the air around the top of the heat sink. This approach offered the advantage of reduced height requirements and enabled the connectors to be centered on one side of the calibration head. Since the wrapped flow configuration was previously unproven, access to simulation was critical in optimizing the design. It would have taken six to eight weeks to build the physical prototype parts, and the cost of computer numerical control (CNC) programming for manufacturing would have been about 20 percent of the overall first-run cost. Consequently, a failed initial prototype design would have led to budget and schedule overruns.

Keysight engineers used simulation to evaluate design alternatives and prove out the cross-flow configuration. The team had been using ANSYS structural and thermal tools, and decided to use this project to evaluate ANSYS CFX software. CFX works within the ANSYS Workbench environment, so it shares the same interface as the structural and thermal tools that Keysight uses. Workbench also integrates well with PTC® Creo® Elements/Direct™ CAD software, which is part of the Keysight toolkit. The CFD technology also offers sophisticated meshing tools, a flexible solver and a variety of physical models, so it handles all of Keysight's fluid-flow simulation requirements.

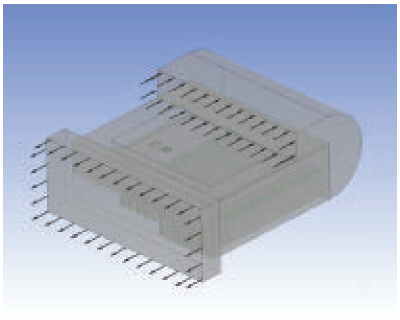
ANSYS COMPUTATIONAL FLUID DYNAMICS SOFTWARE
ansys.com/83CFD

SIMULATING AIRFLOW AND HEAT TRANSFER

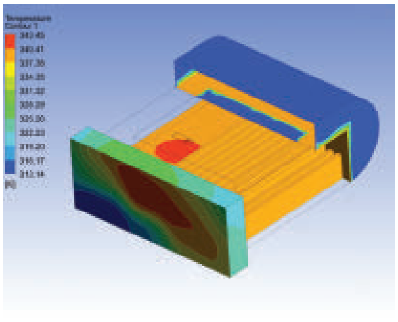
The primary concern of the cross-flow design was that the flow rate of the blower would be reduced due to the pressure drop associated with redirecting the airflow over the heat sink. The blower manufacturer provided a fan curve showing the flow generated at any



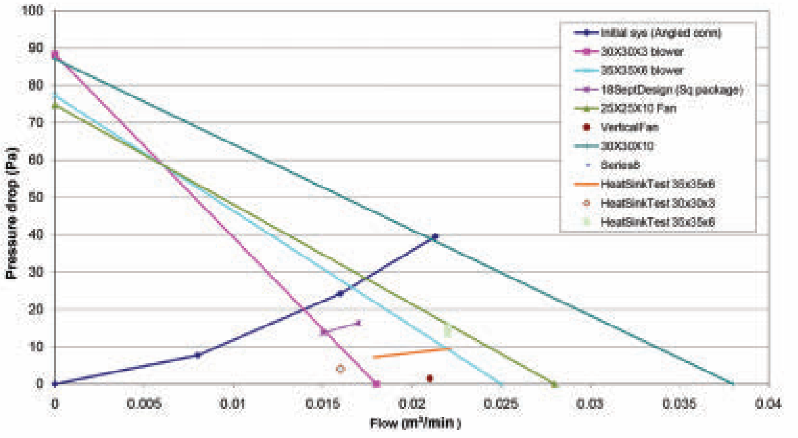
Airflow-only model



Heat transfer model



Heat transfer results



Airflow-only model results

particular pressure drop, but the pressure drop through the calibration head was initially unknown. The team created a proposed design and used CFD to predict the pressure drop at various flow rates. They reasoned that the pressure drop could be reduced by increasing the heat exchanger channel area, so they created a second simulation model.

Simulation results showed that the second configuration did indeed create less pressure drop, resulting in a higher flow rate sufficient to cool the calibration head.

To ensure that this cooling airflow would be sufficient, engineers then built a heat transfer model with 1.5 million tetrahedral elements. The ICs were configured as heat generators, and the conductivity of the housing was based on aluminum. The airflow predicted by the first simulation was used as a mass-flow input. The heat transfer simulation took about 15 minutes to solve on a personal computer; it showed that the case temperature rise was well within the 15 C design specification.

SIMULATION RESULTS MATCH EXPERIMENT

Keysight engineers went one step further by constructing a cross-flow prototype using on-hand parts. Included were a similar heat sink from another project, a blower and a plastic duct. The prototype was constructed to match the latest design configuration as closely as possible. Physical measurements showed that the heat sink rose in temperature by 9.5 C. Keysight engineers modeled the prototype in CFX and ran a simulation to validate the simulation method. The simulation predicted a temperature rise of 9.5 C, a perfect match with the physical measurements. Minor differences in pressure drop and flow between the simulation and physical measurements were within the margin of error of the measurements. These results helped to build confidence in the simulation methodology.

The simulation results helped Keysight engineers to convince management that the cross-flow design would deliver the desired results. Brad Doerr, R&D project manager for Keysight's high-performance oscilloscopes, summarizes Keysight's experience using ANSYS CFX: "Keysight oscilloscope customers demand world-class measurement accuracy to enable emerging technologies. In producing the 90000Q family of oscilloscopes, the Keysight design team needed to develop a superior calibration source to ensure that the product could deliver the industry's highest real-time bandwidth, lowest noise and best jitter performance. In designing the N2806A calibration source, the Keysight R&D team utilized ANSYS CFX software to simulate the environment and optimize the design. As a result, the team successfully produced a highly robust solution that exceeded the requirements for thermal stability, signal integrity and usability. Success was achieved on the first prototype, and this helped Keysight become the first oscilloscope manufacturer to break the 60 GHz real-time bandwidth barrier and enable a new class of ultra-accurate high-bandwidth measurements."

The team successfully produced a highly robust solution that exceeded requirements for thermal stability, signal integrity and usability.

REFRESH YOUR MEMORY

Ooma saved 50 cents on each of hundreds of thousands of devices by using ANSYS tools to design a DDR3 subsystem that does not require a termination voltage regulator.

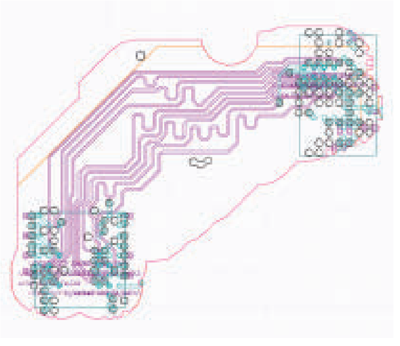
By Michal Smulski, Hardware Engineer, Ooma, Palo Alto, U.S.A.

Consumer electronics manufacturing is all about being first to market with a reliable product at a lower cost than the competitors'. These days, nearly every consumer product contains embedded memory to support the logic core that delivers device functionality. Using low-cost standard commodity memory requires that devices comply with double data rate (DDR) standards issued by the Joint Electronic Devices Engineering Council (JEDEC). The DDR interface consists of signals for control, address, clock strobe and data that are transmitted between the memory controller and DDR dynamic random access memory (DRAM).

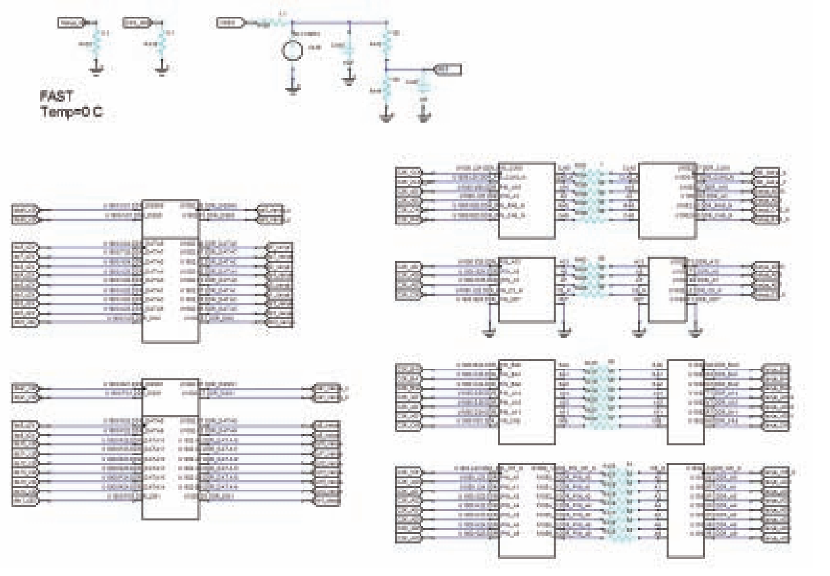
Ooma, which is working to re-invent home telephone service, supports a DDR3 standard on its latest-generation devices that delivers higher performance, but with this performance comes tighter signal integrity requirements for the memory controller. The company's engineers met this challenge by using ANSYS electronic simulation software and tools to simulate performance of the DDR interface in the early stages of the design process, then iterate to an economical solution that avoids the need for a termination voltage regulator.

Consumer electronics manufacturing is all about being first to market at a lower cost than competitors.

Ooma offers consumer and business products that provide free and low-cost U.S. and Canadian telephone calling as well as advanced cloud-based telephony services to its global base of customers. One of the greatest challenges on a recent new product was designing the DDR3 subsystem at the lowest possible cost while getting the design right the first time. The DDR3 subsystem resides on a system-on-chip (SoC) with an ARM microprocessor core. The DDR runs at 533 MHz, and data is clocked on both rising and falling edges for a total bandwidth of 1,066 Mbit per second. The initial concept design was created using Cadence® OrCAD®



▲ Extracted subset of Allegro layout including memory chip, controller and traces, and assigned ports used to model data byte 0 in Designer-SI.



▲ Schematic page for simulation (top). All extracted trace models are placed here and connected to package and buffer models. Each box is an HFSS model of DDR3 traces.

Capture and Allegro® layout tools. Ooma engineers connected the components, generated the net list, routed traces and generated the Gerber files used to fabricate the printed circuit board (PCB).

On slower-running buses, the engineering team sometimes performs signal integrity calculations by hand. But the speed of this bus generated concerns, particularly about timing — the ability of the design to produce a valid signal at the DRAM within the time frame allowed by the specification. Signal integrity was another concern, specifically that parasitics created by the PCB traces might distort the signal. The normal starting point to meet these specifications is to use design rules that specify the geometry of the traces, such as their maximum length and spacing. But with this signal speed, rules of thumb are not sufficient to ensure that the design will work. Allegro offers a signal integrity tool, but Ooma engineers felt it was insufficient for this problem because it lacks 3-D simulation capabilities. Engineers instead used ANSYS electronics tools, which provide a complete timing and signal integrity solution that includes a full 3-D model. Another advantage of ANSYS tools is that the engineering team has the ability to simulate antennas, which are used in an increasing number of Ooma products.

Engineers needed to design the DDR3 subsystem for a new product at the lowest possible cost while getting the design right the first time.

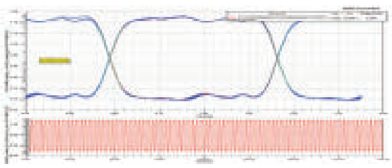
The SoC and memory vendors provided buffer IBIS models and parasitic package models of their products. The interconnect model was directly exported from Allegro to ANSYS DesignerSI via ANSYS ALinks, which streamlines the transfer of design databases from popular third-party EDA tools into ANSYS simulation products. Models for the data, address and control buses were extracted with ANSYS HFSS, an electromagnetic field solver package. The full DDR3 design was created in Designer-SI and simulated with ANSYS Nexxim, a circuit engine for high-speed channel design. The 3-D HFSS model of the interconnects between the controller and memory accounts for capacitance, inductance, coupling, resistance to ground, resistance to power and inductance to power. The design consisted of 40 data, address and controls signals. Ooma engineers generated 3-D models of these signals by grouping them based on trace location and function to limit memory requirements to reasonable levels.

DDR VIRTUAL COMPLIANCE USING ANSYS DESIGNERSI
ansys.com/83DDR

Engineers analyzed the simulation results with the ANSYS DDR Compliance Toolkit to provide a quick verdict on the ability of the design to meet the DDR3 specification. The simulation provided an eye diagram that combined the shape of every possible waveform that could be generated by the design; the diagram is used to visualize and diagnose performance. With this design flow, engineers quickly updated the design — for example, by inputting a different design rule and rerouting the traces — and determined whether or not the new design would meet the DDR3 specification.

The high-speed switching signals used in DDR3 memory generate reflections that cause the signals to overshoot and undershoot the voltage specification, making it challenging to meet design targets. The data signals are terminated in the memory controller, which eliminates reflections on these wires. But there is no internal termination on the control and address signals. Simulation of an early version of the design showed that these reflections would make it impossible to meet the DDR3 specifications. A relatively simple solution is to add a termination

This entire project was completed in a few weeks without involving expensive signal integrity consultants.

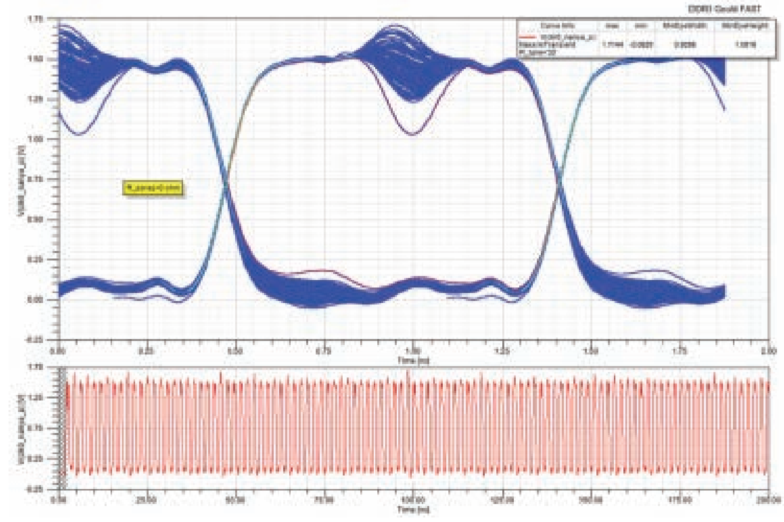


Differential clock eye diagram without series termination

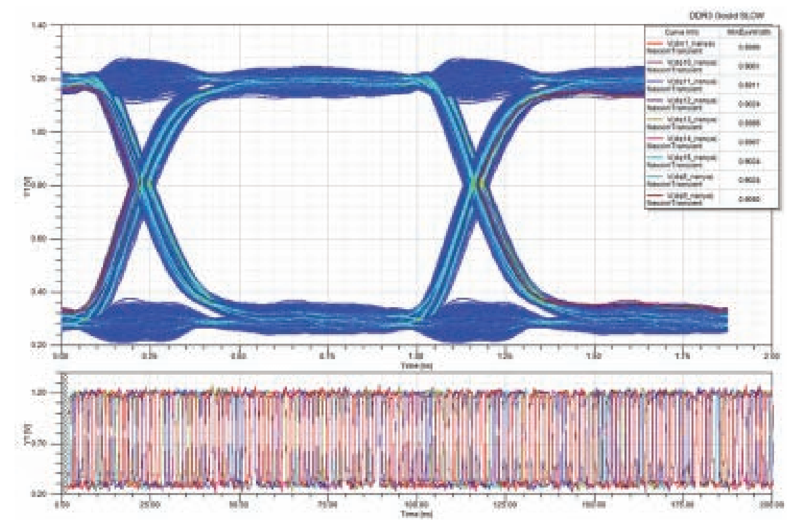
voltage regulator to terminate these wires, at a cost of about $.50. But this is a significant cost when multiplied by hundreds of thousands of units.

To avoid this expense, Ooma engineers tried terminating the control and address lines with an inexpensive series resistor between the controller and memory. The resistor is not as good at controlling reflections as a termination voltage regulator, so signal integrity simulation at various corner cases becomes much more critical. The higher the value of the resistor, the better the job the resistor does in damping the reflections. However, larger resistors tend to round off the leading and trailing edges of the signal, which makes it tougher to meet the timing specification.

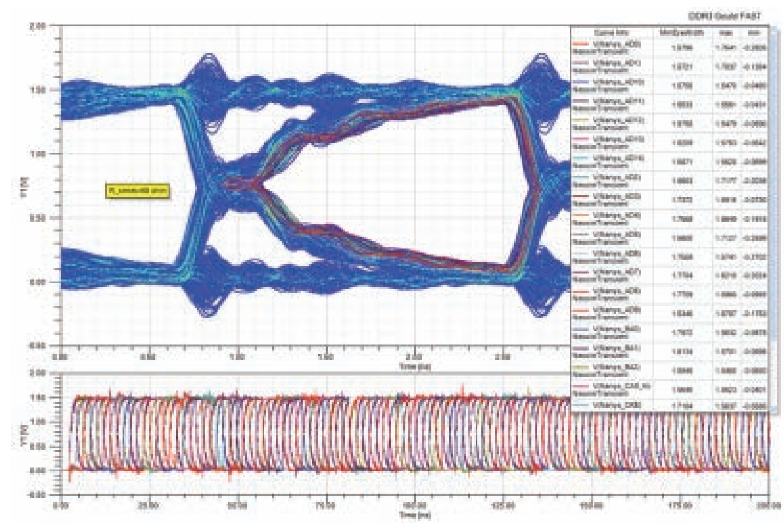
In this case, Ooma engineers swept the value of the resistor from 0 ohms to 100 ohms, while using the simulation to determine the impact on timing and signal integrity. They also made further adjustments in the PCB traces. In the end, the iterated design meets signal integrity and timing requirements without a termination voltage regulator. This entire project was completed in a few weeks by a single design hardware engineer without involving expensive signal integrity consultants. The validated design was then manufactured, tested and FCC certified; it is currently in mass production.



Singled-ended clock eye diagram



Eye diagram of data signal with 60 ohm internal termination



Single-ended DDR3 address and control signals with 68 ohm resistor termination. With this value, the design passed AC overshoot and undershoot specifications.

RF AND MICROWAVE

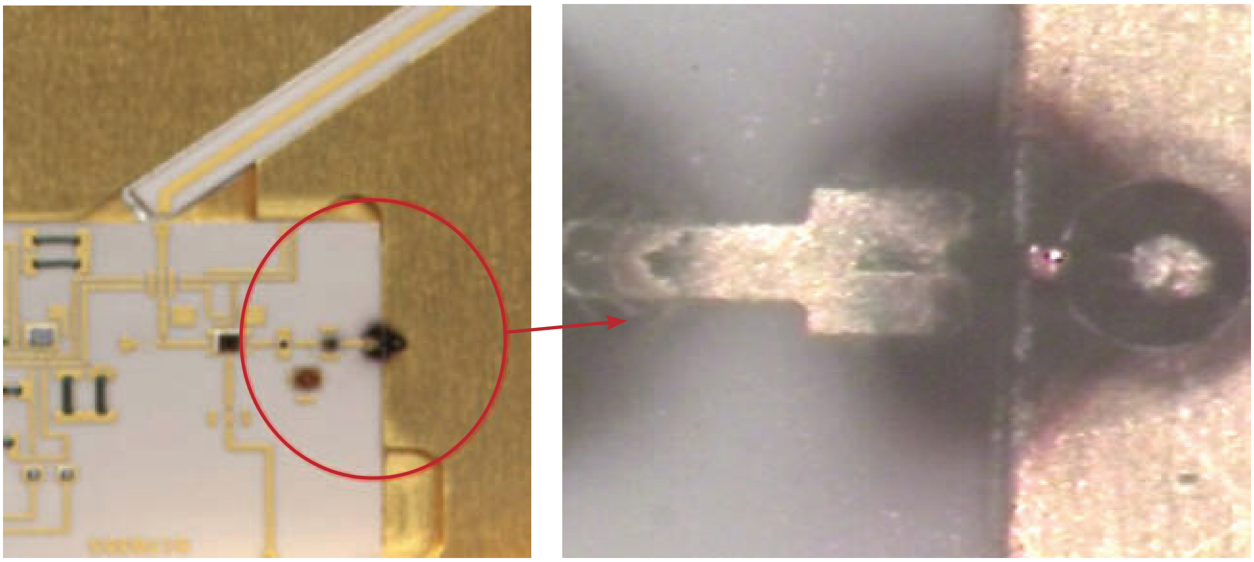
HOT WIRE

Multiphysics simulation helps to achieve robust electronics design for high-power antennas and microwave components.

By Amedeo Larussi
Senior Principal Electrical Engineer
Raytheon Corporation, Goleta, U.S.A.

The aerospace and defense industry is charged with delivering advanced electronics systems faster and at a lower cost than ever before. Antenna and microwave design engineers must balance competing requirements for reduced size, high power delivery, rock-bottom cost and excellent reliability. The result is that antennas and microwave components operate at higher power levels and higher frequencies while being contained in smaller form factors. The inevitable outcome is increased risk that temperatures will greatly impact product performance. Traditionally, electrical design and thermal design are the responsibility of two different groups, each operating

Antennas and microwave components operate at higher power levels and higher frequencies while being contained in smaller form factors.



▲ Photos (normal left, magnified right) show damage to the microwave junction.

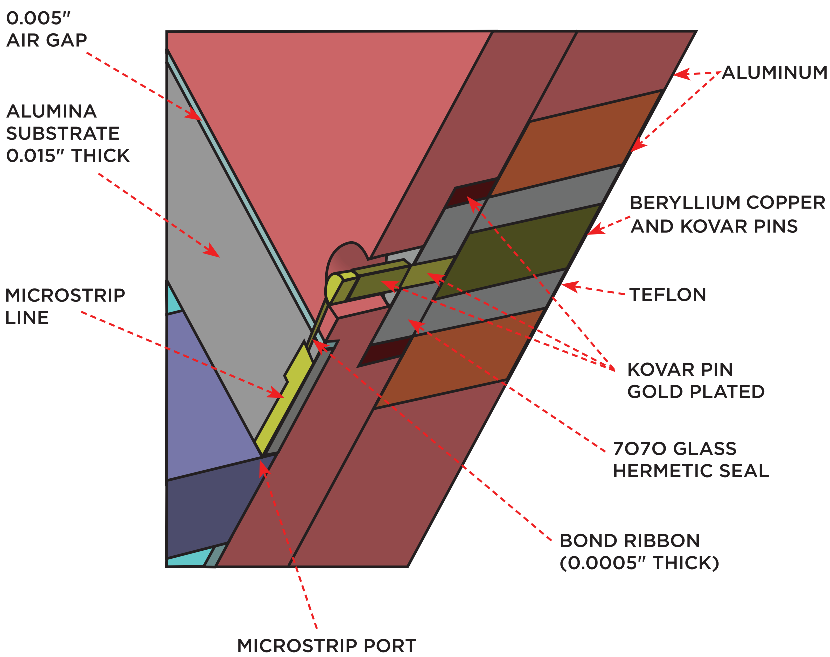
with their own separate requirements and analysis tools — and with only limited cross-group interaction. This common failure to more fully account for design dependencies has, in some documented cases, resulted in serious product malfunctions.

For example, the heat generated by microwave components can increase the dielectric loss tangent of some materials; the consequence is more heat production and the potential for a runaway reaction. In extreme cases, product failure could prevent a mission from being accomplished or even cause loss of life. Combining electrical, thermal and structural simulations often provides unprecedented insight toward preventing failures and improving product performance. Raytheon Corporation — a technology and innovation leader specializing in defense, security and civil markets throughout the world — uses comprehensive robust electronic design solutions to improve the reliability of its products, reduce time to market, and control engineering and manufacturing costs.

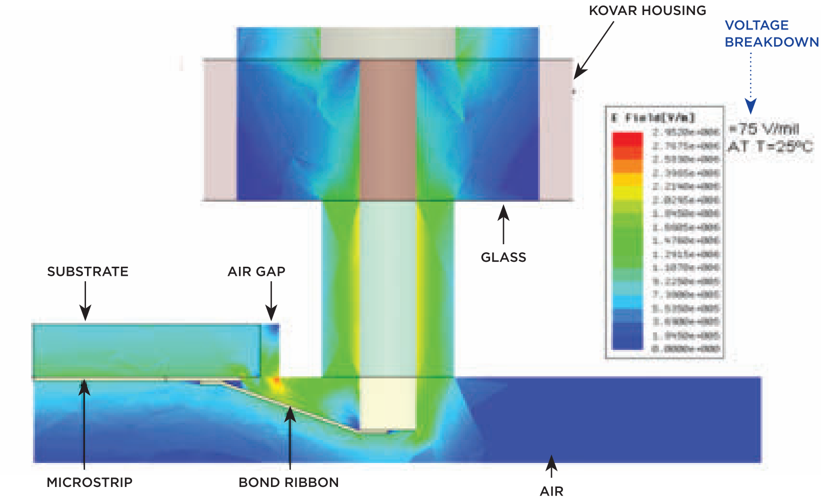
MULTIPHYSICS SIMULATION – A BRIEF HISTORY

Engineers have long been interested in combining high-frequency electromagnetic simulation with thermal analysis, but before the turn of the millennium, there was no efficient way of doing so. About 2002, Raytheon management encouraged investigation into the potential for coupled simulation capabilities. This led to the selection of ANSYS HFSS to enable coupling between electromagnetics and thermal analysis. Raytheon engineers began using the tools extensively to design microwave systems with excellent results. In 2007, the group needed to add vibration and fluid dynamics capabilities to the coupled analysis toolkit. With HFSS integrated into the broader ANSYS simulation portfolio (for example, ANSYS Mechanical and ANSYS Fluent), it was easy and intuitive to perform multiphysics simulations within ANSYS Workbench.

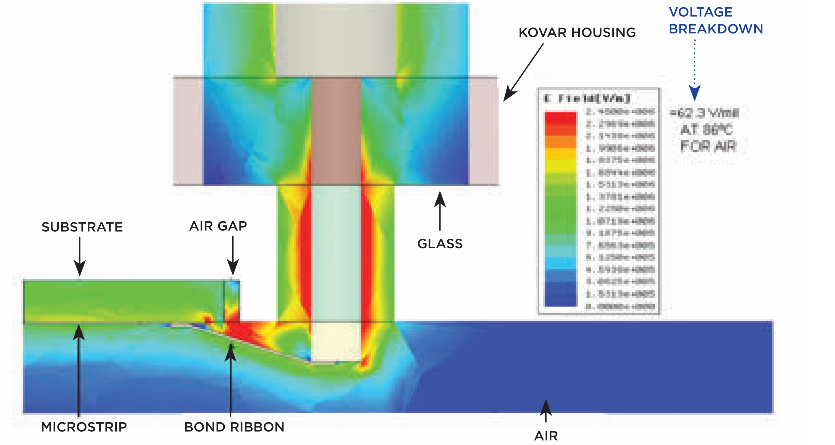
ROBUST ELECTRONIC SYSTEM DESIGN PRACTICES FOR AEROSPACE AND DEFENSE PRODUCTS
ansys.com/83wire



▲ ANSYS HFSS model of microwave junction



Electrical field analysis at 25 C



Electrical field analysis at 86 C

Raytheon engineers took advantage of integration capabilities in ANSYS Workbench to capture electromagnetic and thermal interdependencies.

VOLTAGE BREAKDOWN AT MICROWAVE JUNCTION

In an example from a recent project, a high-power signal is received by the antenna plane. The effective received radiation signal flows to a microwave feed circuit. Although both the electrical and thermal groups signed off on the design, a voltage breakdown occurred at a microwave junction, where a co-axial pin connects to a microstrip trace at the frequency of interest. Shortly after power was turned on, excessive heat destroyed the connector. To address this, Raytheon engineers modeled the components in HFSS. This software accurately models microwave components, such as tuning screws and probes, to a fine level of detail. HFSS employs the finite element method, using small unstructured mesh elements when needed, along with large elements when small elements are not needed, to reduce processing time without sacrificing accuracy. Adaptive meshing refines the mesh automatically in regions in which field accuracy needs to be improved.

Raytheon engineers imported initial design geometry from a computer-aided design (CAD) file. They defined the electrical properties of the materials, such as permittivity, dielectric loss tangent and bulk electrical conductivity for the Kovar® housing, alumina substrate, Teflon® insulator, and beryllium, copper and Kovar pins. Engineers then defined boundary conditions that specify field behavior on the surfaces of the solution domain and object interfaces. They defined ports at which energy enters and exits the model. HFSS computed the full electromagnetic field pattern inside the structure, calculating all modes and ports simultaneously for the 3-D field solution. (The dielectric properties of the materials are temperature dependent.) The HFSS electrical field analysis at 25 C showed that the electrical field in the area in which the failure occurred does not exceed 1.5×10^6 volts per meter (V/m), as compared to the 2.952×10^6 V/m value for voltage breakdown in air.

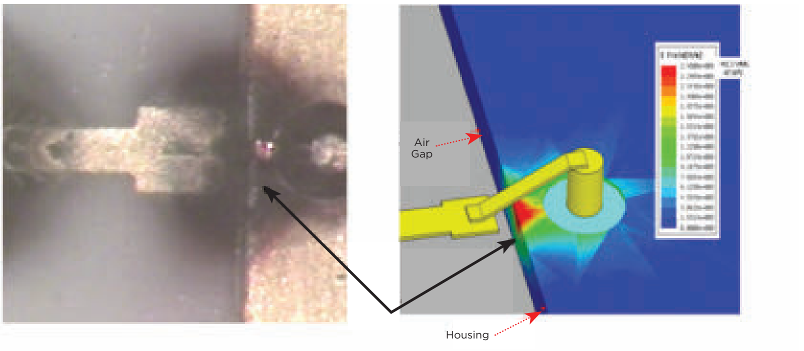
COUPLING ELECTRICAL AND THERMAL SIMULATION

The real-life situation is more complex because ambient temperature affects the dielectric properties of the materials, and the dielectric properties of the materials affect the heat that is generated by microwave components. Raytheon engineers took advantage of the integration built into ANSYS Workbench between HFSS and ANSYS Mechanical to capture these interdependencies. The HFSS model was coupled to ANSYS Mechanical to perform a transient thermal simulation. Boundary conditions for natural convection cooling were added on the bottom face. The temperature distribution was used to perform a static structural analysis.

Engineers employed ANSYS Workbench coupling to apply temperature fields (determined by physical measurements) to ANSYS Mechanical to calculate the thermal stresses associated with these temperatures. The structural simulation showed high stresses and deformation up to 22 µm in the inner connector. Thermal analysis indicated that temperatures actually reached 86 C on the bond ribbon and the pin near the point where they connect, which translated into a lower breakdown voltage. Raytheon engineers re-analyzed the components at 86 C using the dielectric properties at the higher temperature and discovered that the electrical fields in the area where the failure occurred exceeded the $2.45x10^6$ value for voltage breakdown in air at this temperature.

The simulation results helped Raytheon engineers understand how the failure occurred, and they corrected the design to eliminate future failures. The team solved the electromagnetic model at the initial temperature, sent the electromagnetic loss to the thermal simulation to determine the impact of the losses on temperature, sent the temperatures back to the electromagnetic model to calculate losses on the new temperatures, and continued to iterate until steady-state temperature changes were reached. After a few more changes to the materials used in the product, the simulation showed that the design worked perfectly, and this was confirmed by physical testing.

The simulation showed that the design worked perfectly; this was confirmed by physical testing.

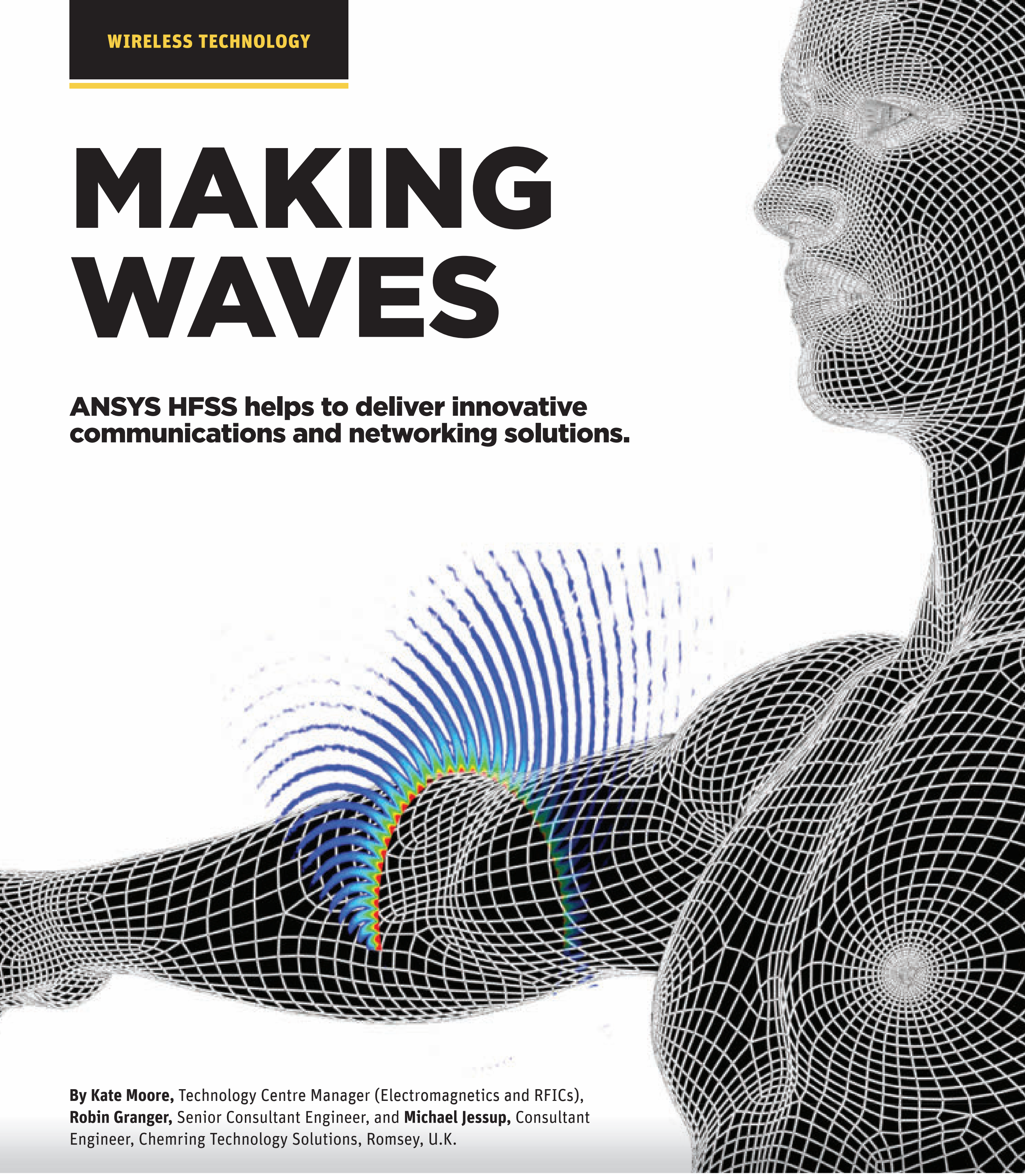


▲ Multiphysics analysis accurately predicts voltage breakdown damage. Physical damage on left and simulation on right. Fields are plotted on the right.

WIRELESS TECHNOLOGY

MAKING WAVES

ANSYS HFSS helps to deliver innovative communications and networking solutions.



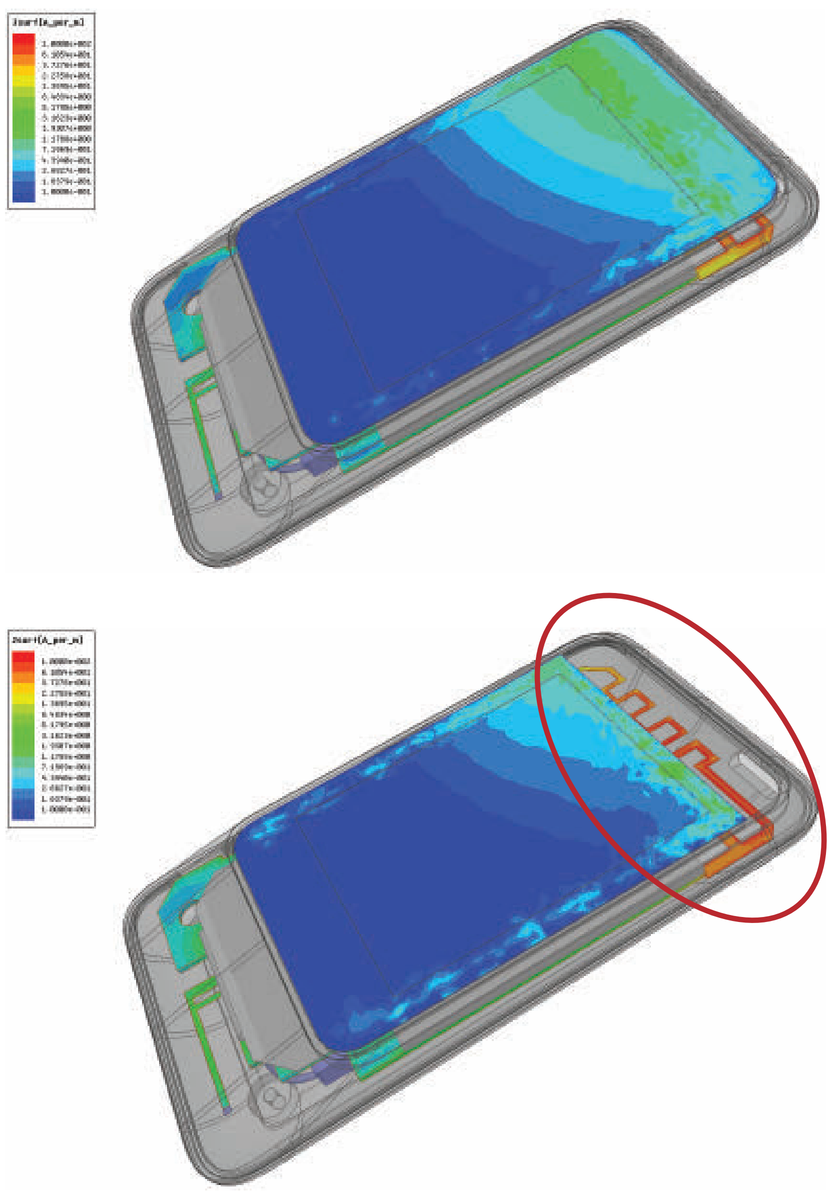
By Kate Moore, Technology Centre Manager (Electromagnetics and RFICs), **Robin Granger,** Senior Consultant Engineer, and **Michael Jessup,** Consultant Engineer, Chemring Technology Solutions, Romsey, U.K.

As industry finds more and wider uses for electronics, electrical engineers must take into account a broad range of factors when designing these smart products — from the environment in which they operate to interference with other electronics to highly original usage of consumer and commercial devices. In ensuring that operation meets and even exceeds expectations, Chemring Technology Solutions' engineers frequently face the challenge of understanding, diagnosing and predicting the behavior of electromagnetic waves as they propagate between antennas, printed circuit board (PCB) traces, packages and other parts of the system. Chemring leverages ANSYS HFSS to simulate the electromagnetic behavior of components and

MODELING TOUCH SCREENS
ansys.com/83screens

▲ SurfLink Mobile wireless hearing aid controller from Starkey Hearing Technologies

Engineers must ensure that device operation meets and even exceeds expectations.



▲ ANSYS HFSS simulation of controller with ITO coating covering full screen (top) predicts 24 percent to 29 percent efficiency. HFSS simulation of controller with upper 8.5 mm of ITO removed (bottom) predicts 66 percent to 70 percent.

systems, making it possible to evaluate many more design alternatives compared to the build-and-test method. The end result is that the team is able to develop more innovative, robust designs in less time than would be possible using traditional procedures.

HEARING AID CONTROLLER

At Chemring Technology Solutions, 400 engineers apply their technical knowledge to solve difficult problems in radar and wireless technologies, electronics and mobile communications, and software engineering across diverse markets, ranging from finance and transport to telecommunications and security. Chemring engineers recently assisted in the design of the SurfLink Mobile® wireless hearing aid controller from Starkey Hearing Technologies. The controller enables two-way stereo audio streaming between a Bluetooth® device, such as a smartphone, and a wireless hearing aid. The greatest challenge was achieving a target of 50 percent radiation efficiency for the device's Bluetooth and 900 MHz radios, the result being that at least half the radio signal power produced by the device is transmitted into the airwaves. Engineers built a rough physical prototype using a 3-D printer, FR4 circuit board material and copper tape; they also simulated the design with ANSYS HFSS. The rough prototype measurements and simulation corresponded well, and predicted radiation efficiency of 80 percent at 900 MHz. But when engineers built a true prototype using actual components, measurements showed efficiency of less than 25 percent.

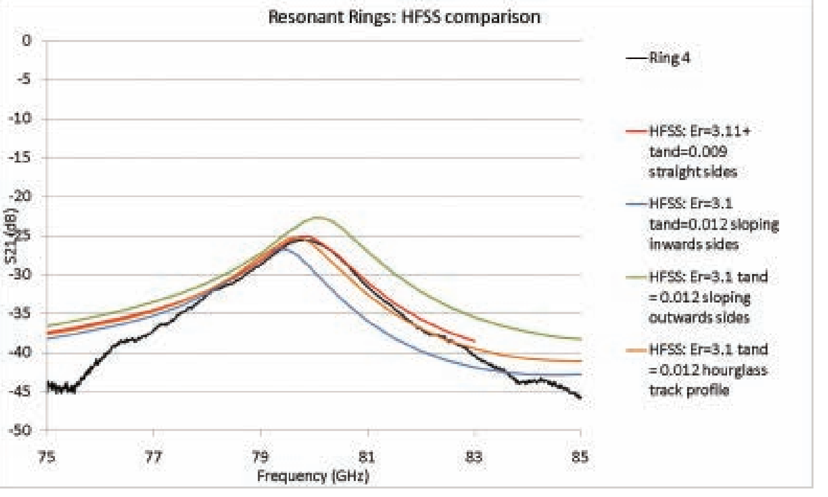
The poor radiation efficiency was quickly traced to the touch screen sensor, which was absorbing approximately 4.5 dB. Engineers noticed that the indium tin oxide (ITO) coating on the touch screen physically extended to the top and bottom edges of the screen, rather than just on the active surface — a parameter that had been assumed in the HFSS model. Engineers made this change to the simulation model, and it showed a drop in efficiency to 25 percent (matching the experimental value and verifying the accuracy of HFSS for this type of simulation). Engineers negotiated partial removal of the coating with the touch screen manufacturer to ensure reliable operation and product integrity. The prototype and updated simulation model showed efficiency of between 66 percent and 70 percent. The SurfLink Mobile wireless hearing aid controller went on sale in fall 2012 and has won numerous awards, including the CES (Consumer Electronics Show) Innovations 2013 Design and Engineering Award.

BODY NETWORK

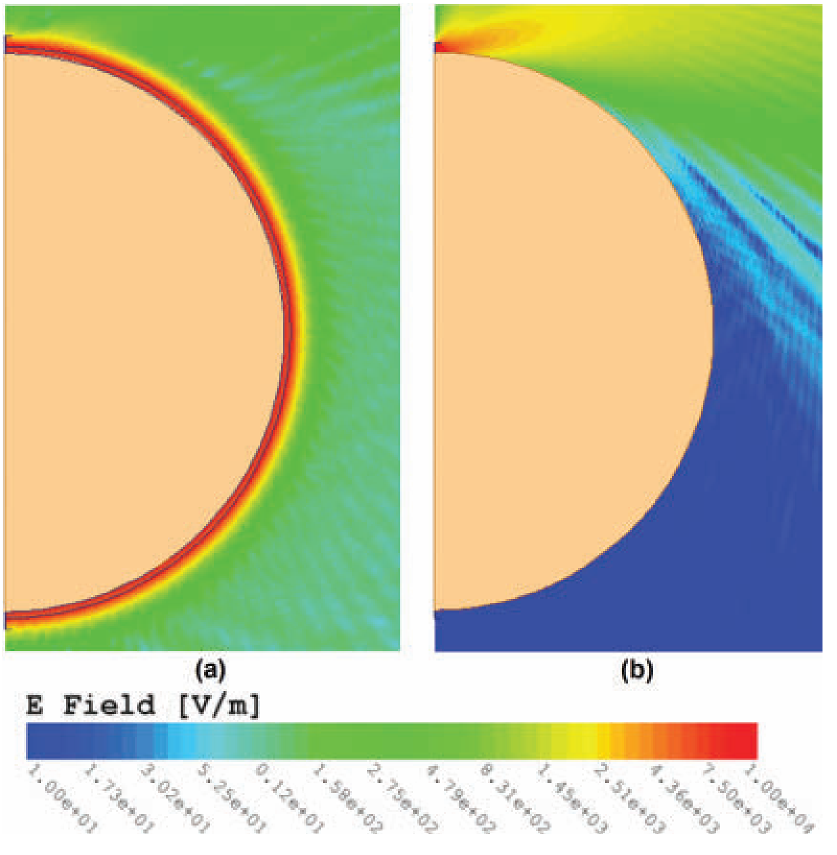
Chemring Technology Solutions' Gekko surface-wave technology is an alternative wireless solution enabling communication between devices over a surface. The signal doesn't travel through a wire; instead, it moves wirelessly over the surface of a fabric that incorporates a dielectric-coated conducting material that creates surface waves that deliver the wireless data. Surface-wave technology combines the reliability, security and performance of a wired system with the flexibility of a wireless system. Gekko overcomes one of the main issues with conventional body networking solutions: the signal's inability to propagate from the front of the body to the back, or around a limb, without the use of repeaters or reliance on reflections. Electromagnetic surface waves follow the propagation surface and provide a channel for secure and robust communications.

Building an effective solution required a solid understanding of surface-wave propagation. In particular, propagation around curved surfaces was not well understood. ANSYS HFSS was used to model surface-wave propagation around curved surfaces and to understand how surface impedance and wavelength can be varied to control the radiation from a particular bend. For example, the team evaluated around-torso propagation by creating a half-cylinder HFSS model with a diameter of 260 mm to approximate a female adult's torso. Wave ports were placed on the opposite sides of the cylinder and used as transmit and receive transducers.

The simulation results showed that the surface wave propagates around the cylinder at 23 GHz and 60 GHz, while a conventional radio signal cannot propagate around the body without use of repeaters. These simulations were used to construct a controlled environment to test the effect of and optimize design parameters before going to the expense of building a prototype. The results also provided a very visual way to inform people of how surface waves work, which is much more effective than a prototype demonstration.



▲ Track shaping makes a significant difference in high-frequency performance.



▲ Simulation of complex magnitude of electromagnetic field over a cylinder representing (a) torso covered with surface-wave garment, and (b) bare skin torso. Losses are much higher in the bare skin torso.

77 GHZ RADAR

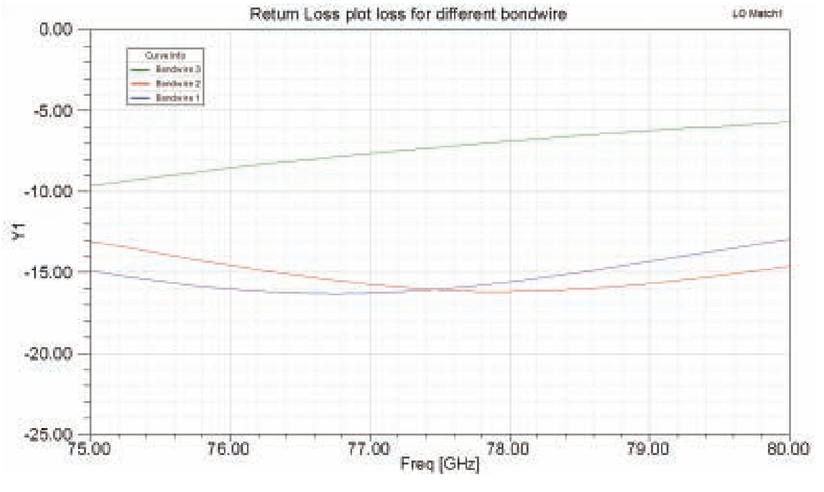
Chemring engineers designing a radar system at the 77 GHz frequency used HFSS throughout the design process of the complete system, which included PCB, IC and antenna. When working with lower frequencies, engineers typically use manufacturers' data sheets to provide important design information, such as the dielectric constant and the loss tangent. But data sheet measurements are usually made at much lower frequencies, so they are not accurate at 77 GHz. To confirm this, Chemring engineers built a simple prototype of the device and used HFSS to simulate it. As expected, the simulations did not match the prototype measurements because the material properties were not valid at 77 GHz.

So engineers adjusted the dielectric constant and loss tangent until the measured results overlaid the simulation at the peak. They had to consider that the as-manufactured traces differ from the perfect design geometry, and at these frequencies these differences have an impact. Engineers used HFSS to change the profile of the traces; this shaping improved the correlation between simulations and measurements. Next, they altered the generic bondwire models in HFSS to match the geometry of the actual bondwires. Again, they saw improvements in correlation. At this point, the HFSS model closely matched the performance of the prototype.

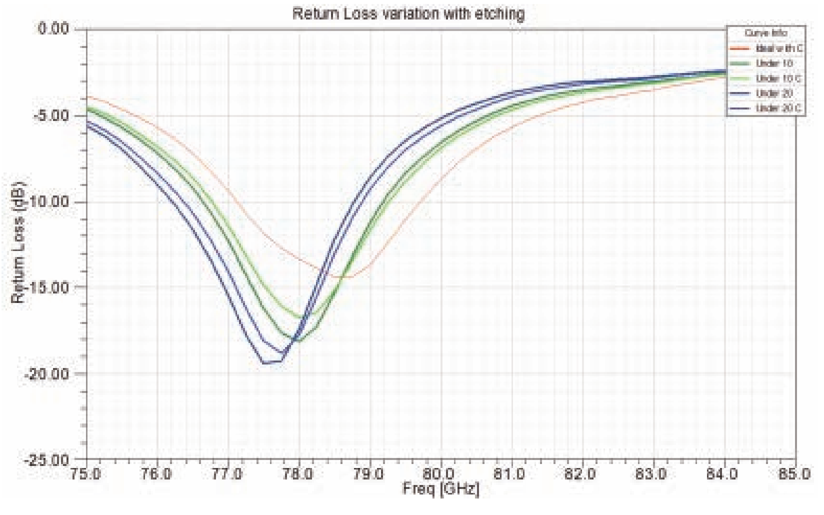
Chemring engineers used the HFSS model to evaluate alternative design approaches and optimize design parameters, such as antenna dimension trace geometry. They then used the model to analyze the effects of over- and under-etching to determine what manufacturing tolerances had to be achieved to ensure final product performance. The result was a substantial improvement in the performance of the finished product and a reduction in the time required to get the product to market.

At Chemring Technology Solutions, ANSYS HFSS plays a key role in most projects involving wireless communications, radar and high-frequency networking in which electromagnetic fields are critical. HFSS automatically generates an appropriate, efficient and accurate mesh for solving the problem. The end result is that Chemring engineers can evaluate as many alternatives as they want in the early stages of the design process. Once the design direction has been determined, Chemring engineers assess the design space to optimize key design parameters. Finally, they often evaluate the sensitivity of the design to manufacturing variation, which saves money in manufacturing and gets the design right the first time.

Engineers can evaluate as many alternatives as they want in the early stages of the design process, then assess the design space to optimize key design parameters.



▲ HFSS predictions for identical circuit with different bondwires for radar system



▲ Parametric simulations show the effects of over- and under-etching, which helps to determine how much manufacturing variation can be tolerated.

MORE GAIN, LESS PAIN

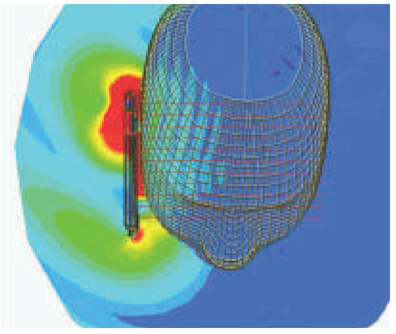
Using simulation, Vortis can design a more efficient cell phone antenna in up to 90 percent less time.

By James R. Johnson, Founder/Chairman, Vortis Technology, Inc., San Carlos, U.S.A.

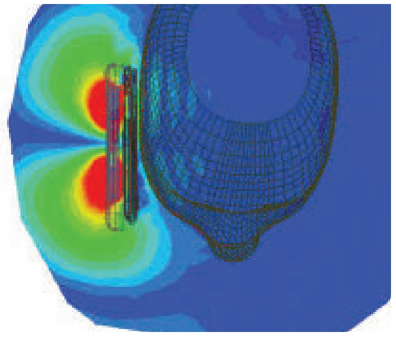
Today's cell phone antennas waste about 50 percent of their power transmitting RF energy into users' heads and bodies. This reduces battery life and produces an annoying buzzing sound in lower-cost hearing aids used around the world. Vortis's new end-fire phased-array cell phone antenna design reshapes the signal pattern so that much less energy goes into the user's head and body. This helps to improve battery life and eliminates the buzzing for hearing aid users.

An antenna that provides the desired figure-eight signal pattern in free space was developed using phased-array theory, but

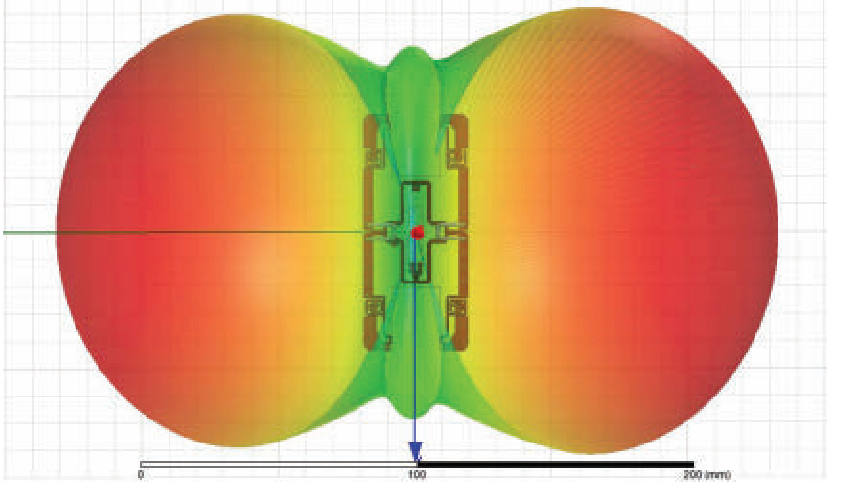
Vortis engineers reduced the time required to customize the design of an antenna by up to 90 percent using simulation.



▲ 2-D radiation pattern of conventional omnidirectional cell phone antenna calculated by ANSYS HFSS



▲ 2-D radiation pattern of Vortis antenna calculated by HFSS . Reduced amount of red at the head indicates a better-distributed signal.



▲ 3-D radiation pattern of Vortis antenna

Vortis engineers have further compressed the design process by using HFSS Optimetrics.

this design must be customized for every phone on which it is used to take into account the effects of the packaging, the cell phone itself and the user's head and hand. Vortis engineers reduced the time required to customize the antenna design for a specific phone by up to 90 percent using ANSYS HFSS. ANSYS Optimetrics evaluated the design space and identified the optimal value for design parameters.

LIMITATIONS OF CURRENT CELL PHONE ANTENNAS

Simple omnidirectional wire antennas that consist of a wire, plated trace or PCB structure sitting on the top, side or bottom of the handset provide adequate performance for most mobile phone applications; they are almost universally used because of their low cost and simplicity. But there are many applications for which these designs are not sufficient or, at the least, higher antenna performance can offer major advantages: industrial and recreational use in fringe areas, devices for the hard of hearing (about 10 percent of the population), and applications in which longer battery life is more important than size.

When cell phones operate, there is a handshake mechanism between the cellular site and the handset. When the signal is strong, the handset reduces energy output to save the battery, and, when the signal is weak, the handset increases power to maintain the connection. As much as 35 percent of the energy radiated by conventional omnidirectional antennas can be absorbed by the head, and as much as 15 percent is absorbed by the hand. This energy must be replaced by increasing the energy output of the phone, which contributes to draining the battery.

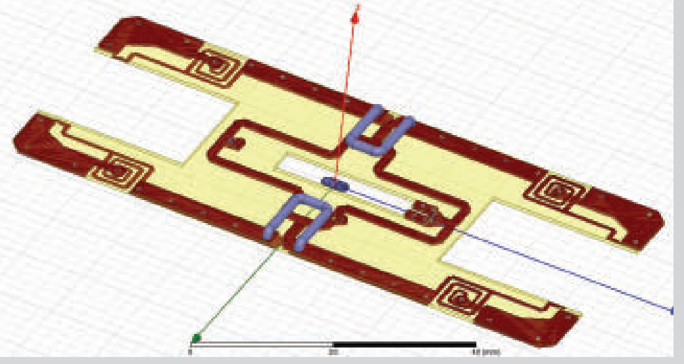
Wearers of hearing aids often experience electromagnetic interference (EMI) problems with conventional omnidirectional cell phone antennas. These antennas radiate a digital pulse that generates currents in the wires in the hearing aid. These currents are amplified by the hearing aid and broadcast by the speaker with a volume to the user of 45 decibels to 85 decibels. The resulting buzz often makes it difficult to use the cell phone and hearing aid at the same time. Most advanced and expensive hearing aids have resolved this under industrial collaborative programs — some with the use of ANSYS HFSS software. However, lower-cost units still suffer from this problem.

NEW ANTENNA DESIGN ADDRESSES THESE PROBLEMS

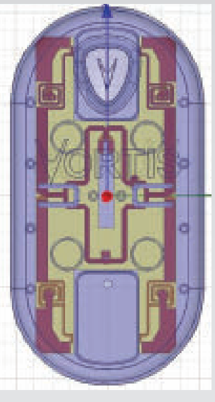
The Vortis antenna overcomes these problems. The end-fire phased-array cell phone antenna radiates a signal in the shape of an eight with deep nulls lateral to the elements and high-gain longitudinal to the elements. The antenna is oriented so that the nulls coincide with the user's head and hand, and the high gain areas enhance the signal forward and rearward of the head to improve the overall uplink.

The efficiency of the Vortis antenna has been tested in free space at 60 percent, which is a 50 percent improvement over the average omnidirectional cell phone antenna. When this number is expanded to incorporate the 40 percent DC to RF energy conversion efficiency typical to handsets, the savings in battery consumption is an estimated 125 percent improvement. This provides 2.25 times more talk time than the traditional antenna. When Vortis is tested against an experimental phantom head, the improvement in efficiency is even greater due to the reduced loss from head absorption. Since the Vortis antenna radiates much less energy around the user's head, the interference to hearing aids is substantially reduced.

PROCESS

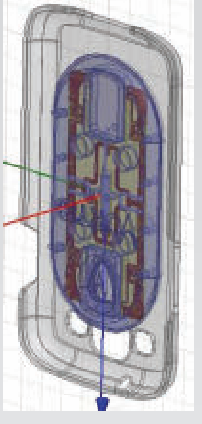


Case I Vortis antenna



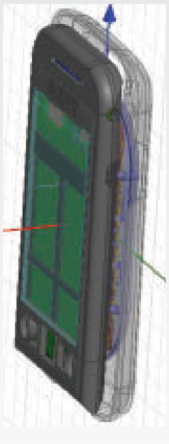
Case II

Vortis + POD (surrounding radome)



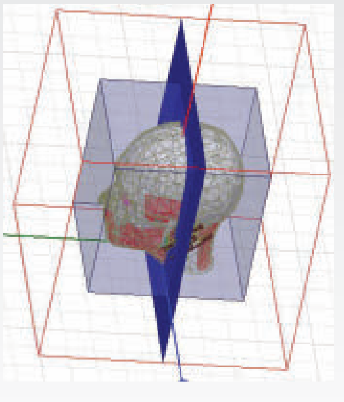
Case III

Vortis + POD + rubber wraparound



Case VI

Phone + Vortis + POD + rubber wraparound

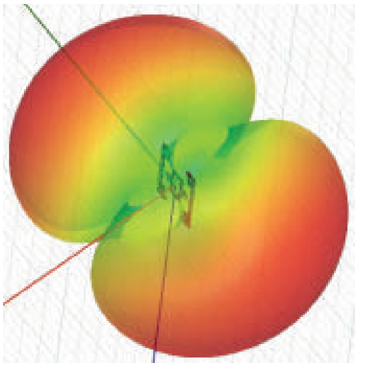


Case V

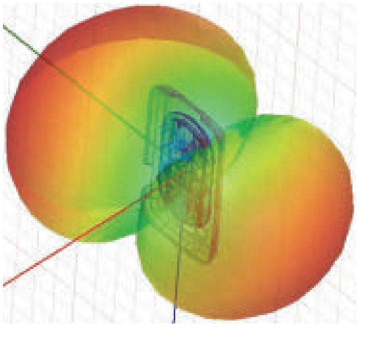
Simulation with phone + Vortis + POD + rubber wraparound + human head

▲ Step-by-step process for using ANSYS HFSS simulation to customize antenna design for specific cell phone

SIMULATION

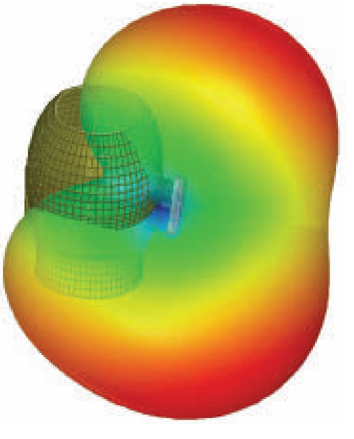


Case I Free space



Case III

Vortis + POD + rubber wraparound



Case V

Simulation with phone + Vortis + POD + rubber wraparound + human head

▲ Simulation results show how figure-eight–shaped radiation pattern was restored at each step of the design process.

When Vortis originally created its concept design, engineers used phased-array theory to create the design of an antenna that would radiate its trademark figure-eight pattern in free space. But in the real world, the antenna design must be adjusted to account for the absorption effects of its package, the phone itself, and the user's head and hand. Therefore, a custom design is required to address individual phone and device requirements with which the antenna is used.

Originally, the company's engineers adapted the design to a new cell phone by building a prototype of the free-space design and testing it with the cell phone and a dummy head and hand. Based on test results, the engineers modified the original design in an effort to recreate the figure-eight pattern under real-world conditions. They then built and tested a prototype. Each design iteration cost about $5,000 and took about one week. An average of 10 design iterations were required to create a satisfactory custom design for a typical application, so the costs were about $50,000, and the lead time was 10 weeks, potentially making the process 10 times faster and easier.

SIMULATION REDUCES DESIGN COST AND TIME

With more design variables and tighter schedules, simulation is the only means to meet today's design requirements. A year ago, Vortis began using ANSYS HFSS simulation to adapt its antenna design for specific cell phones. Engineers began by using ANSYS ALinks for MCAD to import the geometry of the Vortis antenna, antenna package, rubber wraparound (sometimes used to connect the antenna package to the cell phone), cell phone and ANSYS human head model. Engineers began with the basic free-space antenna design and added the antenna package, reran the simulation and noted how the radiation pattern was distorted. They adjusted the antenna design and, in the course of several iterations, restored the original figure-eight pattern. Next they added the rubber wraparound and cell phone to the model geometry. They reran the simulation and noted the resulting distortion in the radiation pattern. They created and simulated additional iterations to remove the distortion. Finally, they added a head and a hand to the model and went through the same process.

Recently, Vortis engineers have further compressed the design process to a single step by adding all of the elements that need to be considered in the beginning of the simulation process and then using the Optimetrics parametric analysis tool to generate a designed experiment consisting of a series of iterations to explore the complete design space. The design parameters used in this experiment were those that had been shown in earlier simulations to have the greatest effect on the radiation pattern. The design of experiments results were used to estimate the value of each relevant design variable that would produce the best fit to the desired figure-eight pattern.

Using HFSS and Optimetrics, Vortis can create a customized antenna design for a specific cell phone in one-tenth the time and cost required with the build-and-test method.

Using HFSS and Optimetrics, Vortis can create a customized antenna design for a specific cell phone in only about one-tenth the time and cost required with the build-and-test method.

ANSYS HFSS FOR ANTENNA SIMULATION
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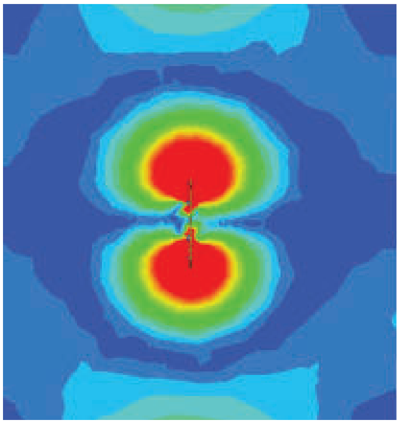
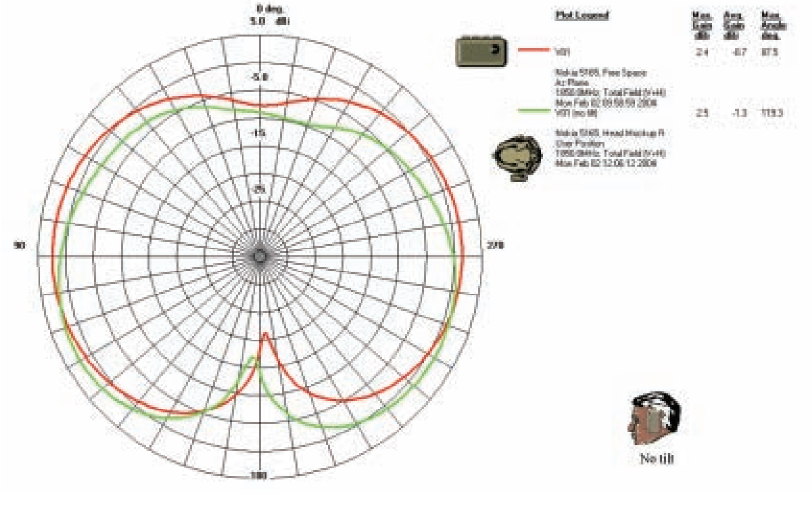


▲ Antenna radiating energy looking top-down in near fields



▲ Test results confirm simulation accuracy.

MANAGING IP RISKS

IP-aware SoC power noise and reliability analysis workflow is required in the FinFET era.

By Karthik Srinivasan, Corporate Applications Engineer Manager, Analog Mixed Signal, ANSYS

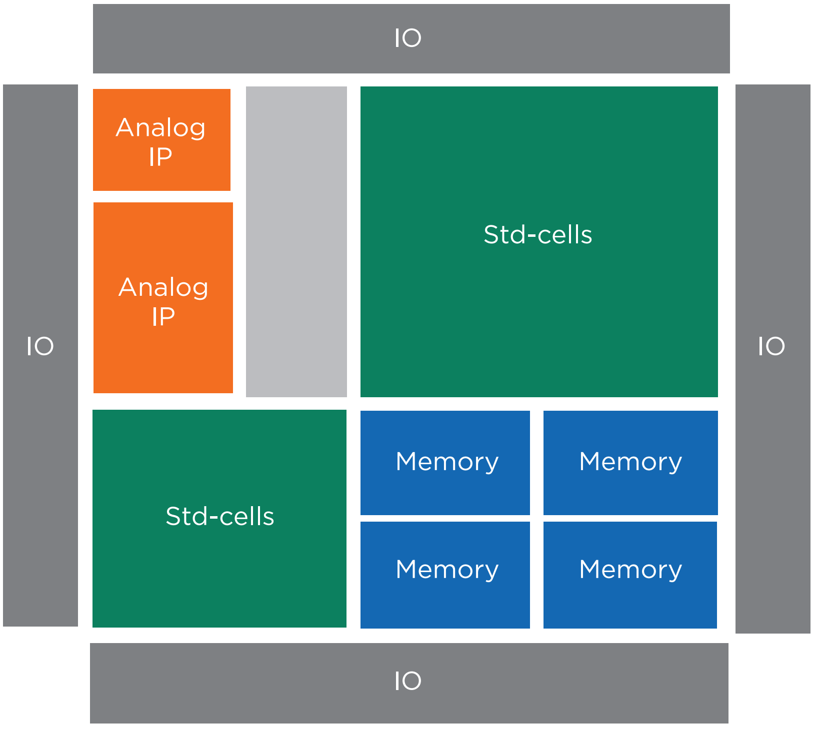
One of the biggest benefits of system-on-chip (SoC) designs is that they are modular and build upon previously validated intellectual property (IP) components, either developed in-house or purchased from external sources. This approach enables SoC engineers to quickly create new designs and shorten time to market. But, because engineers who are designing the individual components are often not the ones who are designing the SoC, challenges arise during full-chip verification. The IP and SoC designers may have different expectations with regard to the conditions for final sign-off. If the gap in

IP and SoC designers may have different expectations with regard to the conditions for final sign-off.

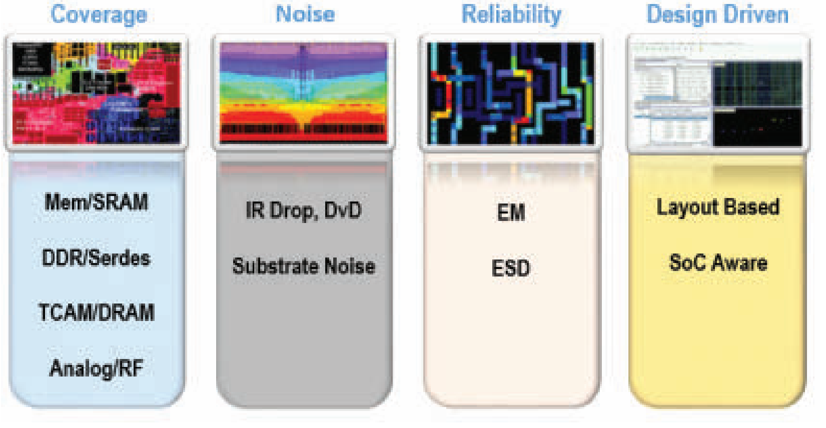
expectations is large, it can create design issues that affect the final product's performance, functionality and release date.

IP engineers often validate their designs as if each component were operating in near-ideal conditions. SoCs are verified and signed off with mainly abstracted or, in many cases, black-box views of the IPs. However, as more and more high-speed and noise-sensitive components get placed next to each other, or next to the core, digital logic failure conditions emerge that once were not considered. This worsens when these IP components share one or more power and ground supply domains. For example, when a bank of high-speed DDR interfaces is placed next to a bank of memory, the switching of the DDR can generate sufficient noise on the shared ground network to adversely affect memory operation.

As designs migrate to smaller silicon technology nodes, especially 3-D transistors or FinFET, differing design goals for IP and SoC designers will adversely affect power noise and reliability. When the supply voltage is scaled down from 1+V levels to the sub-700 mV range, fluctuations that had been between 5 percent and 10 percent increase to about 15 percent to 20 percent because of a combination of higher peak current, increased current density and reduced supply voltage levels. Thus, the impact of power noise becomes more significant for FinFET-based designs than in earlier technology. Accurate prediction of these fluctuations in the power and ground network is critical to ensure that IP components continue to operate as designed in the full-chip context. The traditional divide-and-conquer approach of over-design doesn't work when on-chip resources become scarcer and noise coupling increases due to the presence of multiple voltage islands. Design and verification of IP components for power noise immunity requires a two-step approach.



▲ Typical SoC architecture with multiple IPs

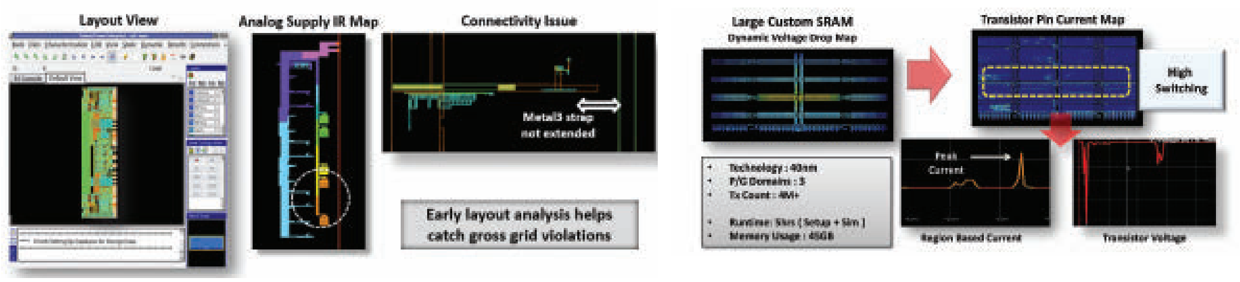


▲ Requirements for a successful IP power noise verification environment

LAYOUT-BASED DESIGN ANALYSIS

As a first step, the IP itself needs to be simulated extensively during the design process to ensure that the power distribution network and signal interconnects are as robust as possible. For this particular step to be successful, the methodology should be applicable to any type of component but with some differences based on each type. In addition, the approach must support many different analyses and needs within a single environment; these include static and dynamic power noise modeling, substrate guard ring design verification, power- and signal-line electromigration sign-off, and electrostatic discharge integrity verification. Because of the customized nature of these designs, the simulation environment should be layout driven. In contrast to typical SPICE-based simulation approaches that are difficult to analyze, the results should be overlaid on the layout to enable quick in-design fixing and iteration.

A layout-based approach highlights design weaknesses quickly through static and dynamic simulations. The connectivity and static IR simulations must be performed early in the design process to identify and fix gross grid issues. As the design matures, dynamic voltage drop analysis can be used to isolate specific



Layout-based power and reliability verification from early phase to sign-off for custom and analog IPs. This approach highlights design weaknesses quickly through static and dynamic simulations.

Accurate prediction of fluctuations in the power and ground network is critical to ensure that IPs continue to operate as designed.

areas of the design that are likely to fail from simultaneous switching.

The simulation environment should be SoC-aware so that the IP designer can include the impact of the SoC-like switching noise coupling, power-ground grid impedance and package parasitics easily into runs without compromising the turnaround time and required simulation efficiency. An ANSYS-based framework can enable such an SoC-aware IP analysis and sign-off methodology.

ACCURATE MODELS WITH EMBEDDED RULES

The second step involves creating accurate, representative and compact models of the IP component that not only capture the physical and electrical attributes but also incorporate embedded rules. These models can be plugged into the SoC analysis to ensure that the IP obtains a robust power-ground connection and model its impact on other parts of the design. The embedded rules

IP-SOC INTEGRATION FLOW
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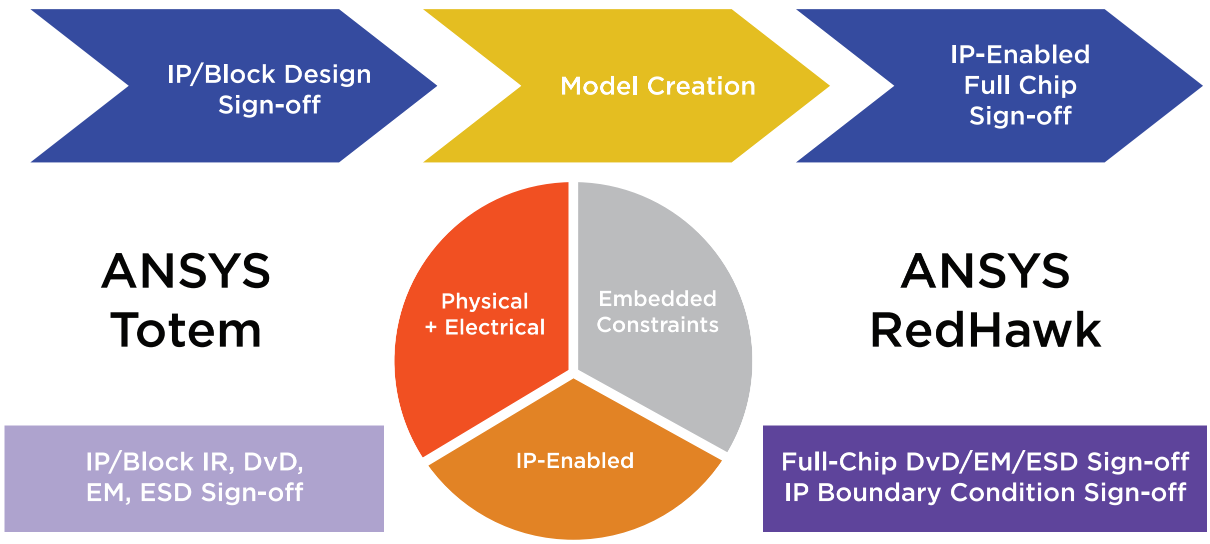
provide a straightforward mechanism to check whether or not the connectivity of IP at the SoC level meets the expectations of the designer.

As designs move to 14 nm technologies based on FinFETs, power noise and reliability become the top concerns. This is especially true for IP components, as they involve multiple parties and design steps leading to increased chances of failure. Having a robust validation methodology that also incorporates a model creation and model use framework using ANSYS Totem and ANSYS RedHawk will enable both IP and SoC designers to meet future challenges.



Full chip sign-off with accurate IP macro models

OVERCOMING UNCERTAINTIES IN HIGH-SPEED COMMUNICATION CHANNELS

ANSYS HFSS helps verify the ability of cost-effective laminates to support communications speeds of 10 gigabits per second or greater.

By Rick Rabinovich, Senior Principal Design Engineer
Alcatel-Lucent Enterprise, Calabasas, U.S.A.

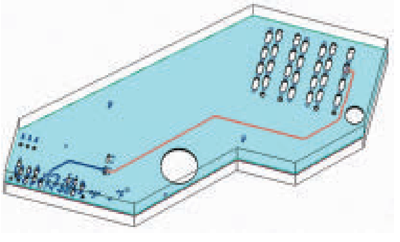
Each new generation of networking products delivers higher performance than the last — at equal or lower cost. Engineers tasked with designing high-speed communications channels for these products face a difficult challenge. The increased uncertainties involved in system performance at speeds of 10 Gb/s and higher encourage engineers to design for higher safety margins by choosing more sophisticated printed circuit board (PCB) laminate materials despite the higher costs. On the other hand, competitive pressures place a premium on the use of the most cost-effective materials and components, which may create uncertainties in product performance, possibly forcing a redesign at great expense after the hardware becomes available.

Engineers at Alcatel-Lucent Enterprise — a leading provider of products and innovations in Internet protocol (IP) and cloud networking, as well as ultra-broadband fixed and wireless access — addressed this challenge by using ANSYS HFSS to evaluate the performance of different materials and components in the early stages of the electronic design process. As an example, engineers extracted simulation channels from the post-layout database of two boards, concatenated them, and ran simulations in the frequency and time domains. They used

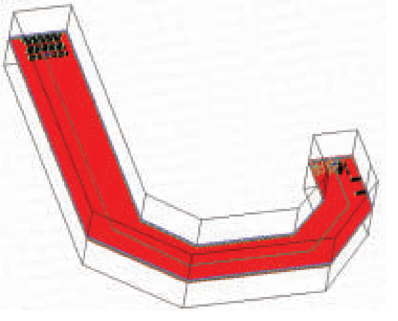
HFSS to determine the lowest-cost solution to reliably link integrated circuits (ICs) on two separate boards across a 12.5 Gb/s channel.

The channel links two boards, A and B, through an inter-board connector. During the initial concept design, relatively low-cost board materials were selected. Board A comprised an enhanced FR4 material that held the serializer-deserializer (SerDes) transmitter and a 3.3-inch differential channel that connected one IC to the connector. The channel started at the IC and extended about 0.5 inch on the top surface until it transitioned to layer 3 to reach its final destination at the connector. Board B comprised Megtron 4 material holding the SerDes receiver IC and an 11-inch differential channel that connected its IC to the connector.

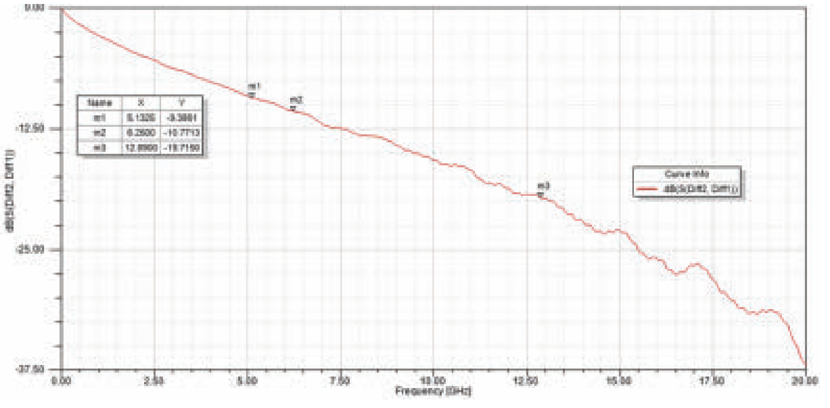
The project's simulation objective was to verify that a 12.5 Gb/s channel can reliably link two ICs located on two separate boards connected with a high-performance connector. The design specified that the frequency domain insertion loss (IL) must increase monotonically until its Nyquist frequency of 6.25 GHz without exceeding 20 dB, and the return loss (RL) must stay above 12 dB up to 6.25 GHz. In addition, the design needed to achieve stringent time-domain performance. The bit-error rate (BER) should be 10 to 22 or better after the signal has passed through the analog equalizer and decision-feedback equalization (DFE) filters located in the SerDes receiver IC.



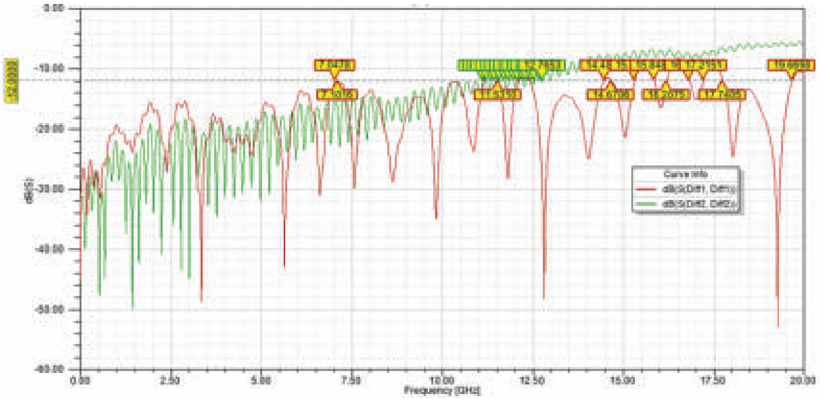
▲ Board A



▲ Board B



▲ Insertion loss simulation



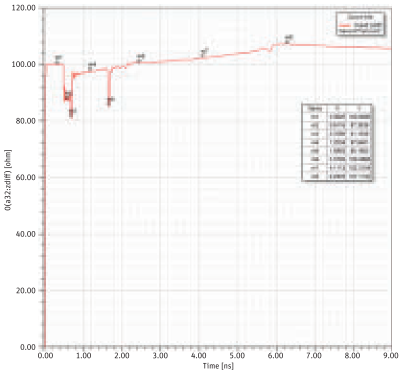
▲ Return loss simulation

FREQUENCY DOMAIN SIMULATION

Alcatel-Lucent engineers used ANSYS Designer and ANSYS HFSS to simulate this channel. The simulation started by building a frequency domain model in HFSS that was ported into Designer to analyze the structure performance in the time domain. This process provided more accurate results than the competitive approach of starting with a time-domain model. In Designer, engineers extracted the channel on each board from the post-layout database using the cutout sub-design function. They verified the stackup, edited the cutout to eliminate incidental shapes that extend the simulation time, and created the port excitations. Then, they ported the structure to HFSS to account for the copper surface roughness and to generate a higher-fidelity model.

Engineers then ran the frequency-domain simulation and verified that each board met the expected frequency-domain specifications. They generated a four-port S-parameter channel model of each board in HFSS. After creating a circuit schematic in ANSYS Designer, they imported the models of the two boards and the connector model provided by the manufacturer, and concatenated them to simulate the IL and the RL of the complete channel. The results showed that the IL was 10.7 dB and RL was above 12 dB up to 7 GHz. Both of these simulations met IL and RL requirements.

ANSYS HFSS 3-D LAYOUT
ansys.com/83layout



TDR simulation

HFSS 3-D simulation confirmed with a high degree of certainty that the channel will operate properly and meet frequency- and time-domain specifications.

TIME-DOMAIN SIMULATION

Next, engineers created a circuit with a single instance of the concatenated channel and used the time-domain reflectometry (TDR) probe built into Designer to visualize the impedance profile of the channel under test. The impedance discontinuities are responsible for increased IL, RL and closure of the eye. The results showed the expected profile of a three-inch board, connector and 11-inch board. The simulation results also showed an impedance discontinuity on board A that represented the trace transitioning from the top to the inner layer in the layout.

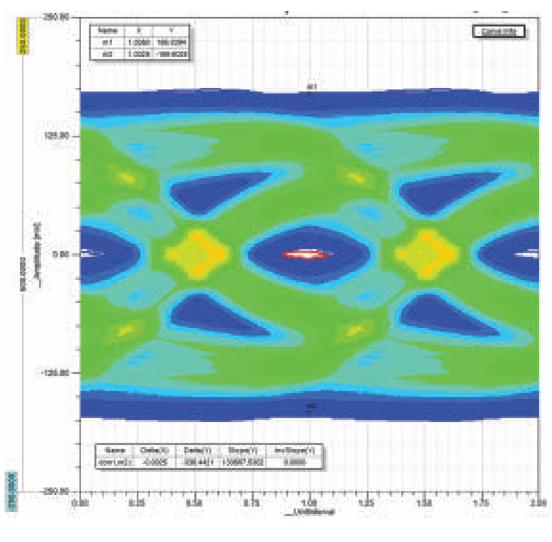
EYE DIAGRAM SIMULATION

Engineers then created a circuit to run the eye diagram (eye mask test) simulation. They used the same single instance of the four-port S-parameter model of the complete channel used in the TDR simulation and added the IBIS-AMI models of the transmit-and-receive SerDes provided by the IC manufacturer at each end of the channel. Using ANSYS Designer, the IBIS-AMI register settings were configured to maximize the opening of the eye.

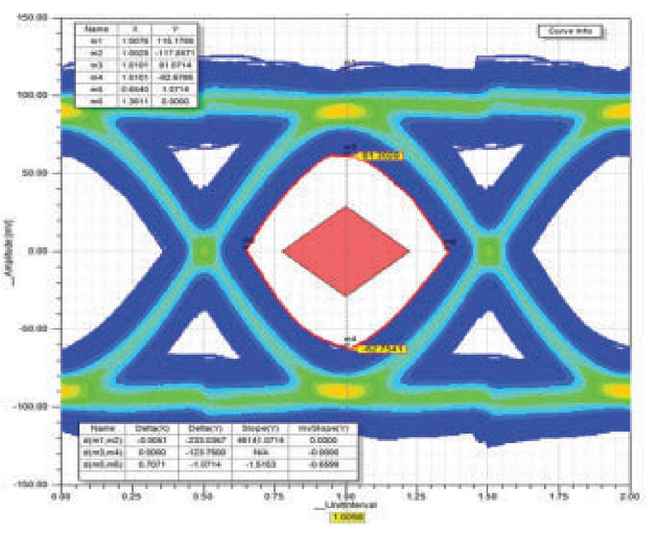
Engineers measured the eye diagram at the receiver IC after the built-in analog receiver and DFE filter. Even though the display showed a closed eye at the receiver IC pad, the continuous-time linear equalizer (CTLE) and DFE filters at the receiver opened the eye within the silicon. The filtered signal eye mask correlated to a BER better than 10 to 22. Therefore, the simulation results indicated that the channel was also compliant in the time domain.

Designer and HFSS's powerful combination of frequency- and time-domain analysis enabled Alcatel-Lucent engineers to remove the uncertainties of the trade-off between performance and cost. The HFSS 3-D simulation confirmed with a high degree of certainty that the channel will operate properly and meet frequency- and time-domain specifications. The results showed that a reliable product can be built with less expensive materials and connectors and will still exceed the BER objective. Engineers also verified that the channel meets the IL and RL frequency-domain specifications. As a result of this work, Alcatel-Lucent engineers were able to reduce PCB costs by 67 percent and achieve 5 percent savings in the overall cost of the system while avoiding the risk of expensive late-stage design changes that disrupt the project schedule.

Thanks to David Choe of ANSYS for his mentoring, great technical knowledge, familiarity with the tools, and patience while demonstrating the use of ANSYS Designer and ANSYS HFSS. Thanks also go to Michael Nisenson at ANSYS for his continuous and steadfast support.



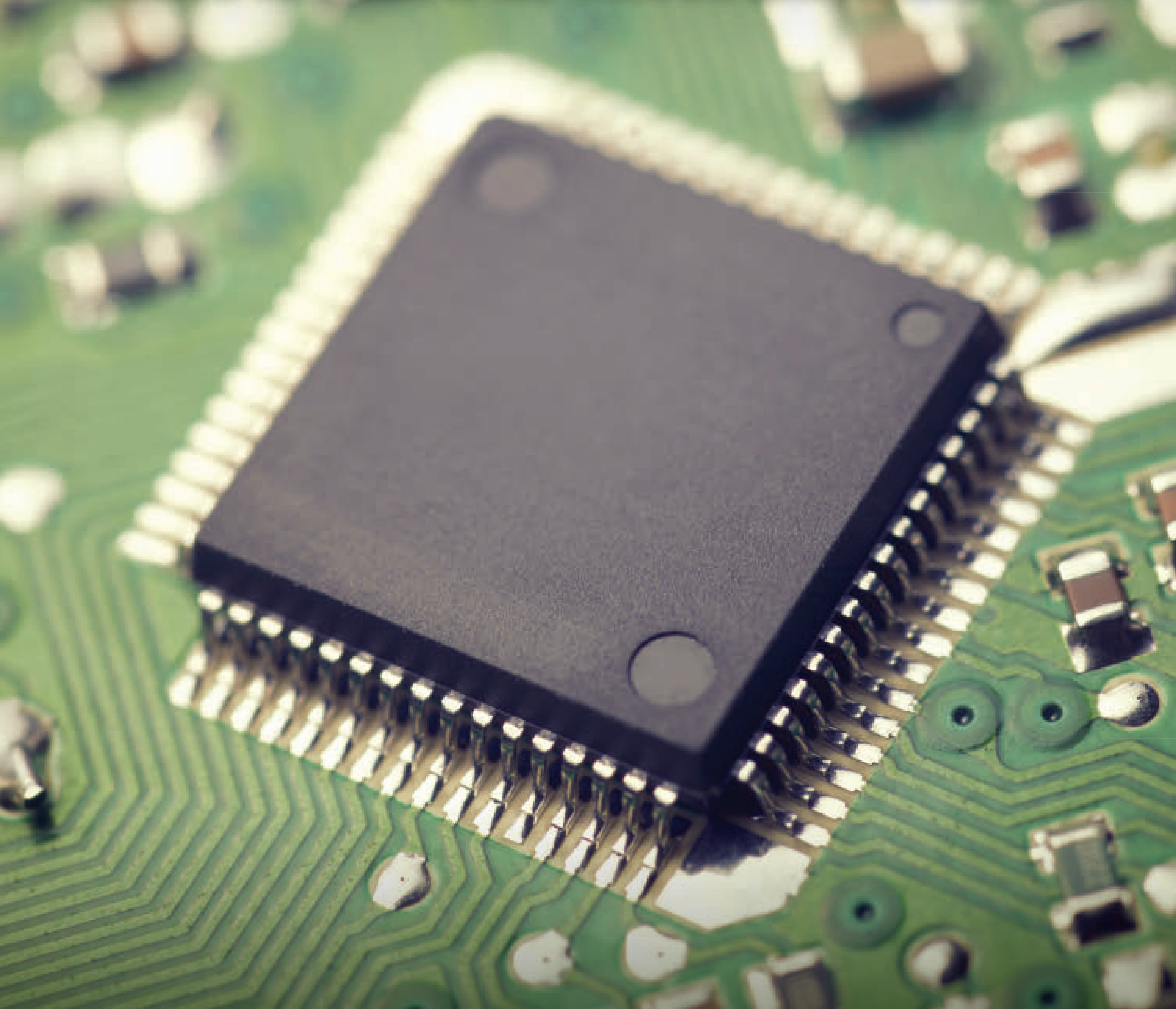
Simulated signal at receiver



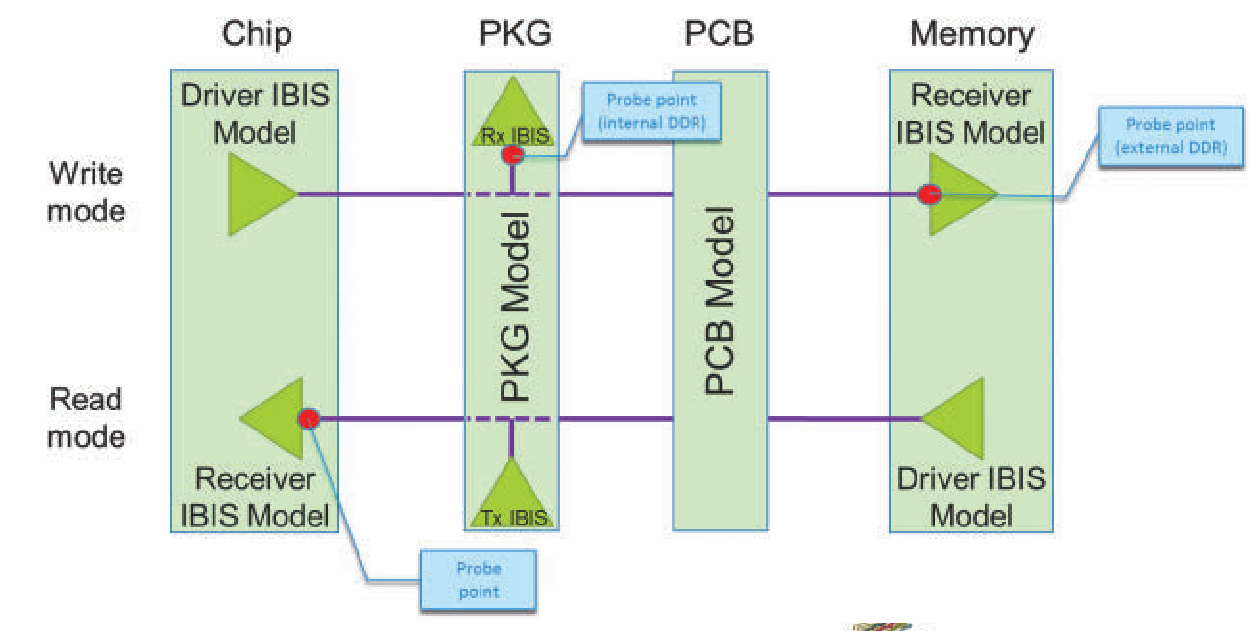
Eye mask simulation shows signal after RX equalizer and DFE.

MAINTAINING POWER AND SIGNAL INTEGRITY

The ever-changing hardware that supports big data and the Internet of Things must be fast, reliable and quickly developed.



By Larry Zu, President, Sarcina Technology LLC, Palo Alto, U.S.A.



Bidirectional channel simulation environment for SiP package

Every few years, a new electronic invention changes our lives. These devices and services rely on powerful data centers, which demand robust chips as well as high-speed interconnects and input/output (I/O). Accordingly, the printed circuit boards (PCBs) must be powerful and well-designed to provide quality solutions for power integrity and signal integrity. Additionally, all connectors and electrical and optical cables connected to the PCB must provide a reliable environment for high-speed digital signals.

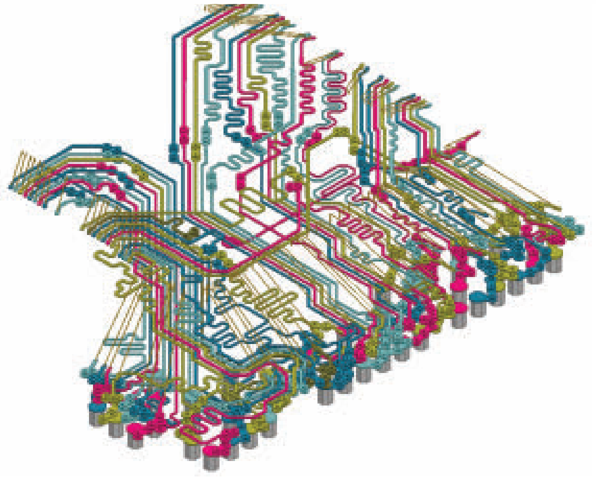
To keep pace with big data and the Internet of Things, PCB/chip speed and reliability are paramount. To meet aggressive specifications, engineering teams need accurate simulations to validate and improve designs before they are taped out — and well before prototyping.

Sarcina Technology has expertise in designing high-performance, application-specific integrated circuits (ASICs) and their PCBs. The company employs state-of-the-art simulation tools from ANSYS for these challenging tasks.

TO SIMULATE OR NOT

Simulation software gives engineers the ability to do amazing things. However, having that capability may require a significant outlay of funds for both software and necessary engineer training. This raises the question: Is simulation software worth the increased non-recurring engineering cost?

Electrical simulation software gives designers all the tools needed to successfully design complex products the first time, every time. For instance, electronics developers at Sarcina Technology use the ANSYS HFSS 3-D full-wave solver for modeling because of its accuracy and reliability. An organization can use a variety of factors — including competition, price, profit margin, design constraints and system intricacies — to determine if simulation software is the right choice.



3-D view of LPDDR package model

To keep pace with big data and the Internet of Things, PCB/chip speed and reliability are paramount.

ANSYS HFSS 3-D LAYOUT
ansys.com/83power

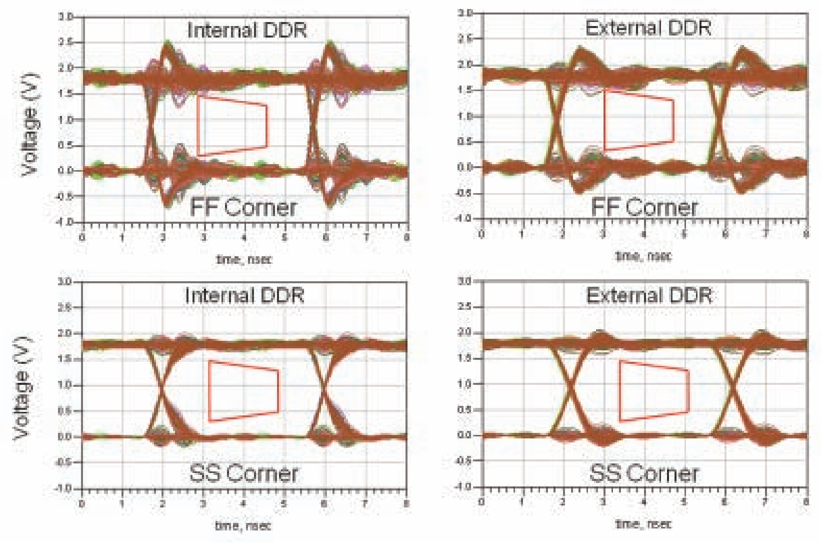
BIDIRECTIONAL CHANNEL FOR SYSTEM-IN-A-PACKAGE (SiP)

The ASIC chip inside an SiP can communicate with either the internal low-power double data rate (LPDDR) die inside the

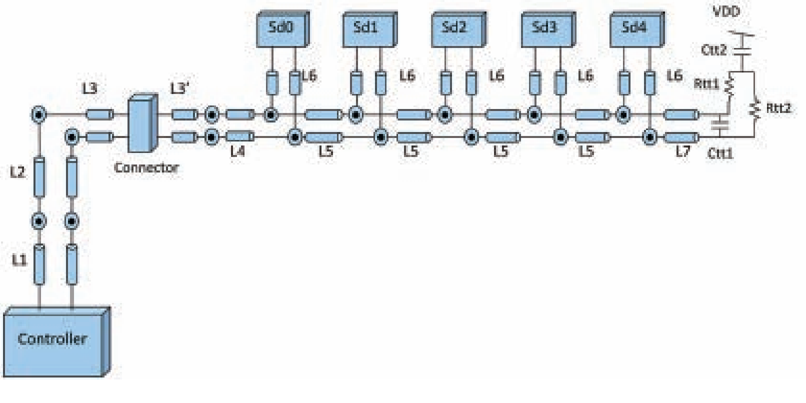
SiP or an external LPDDR memory chip on the PCB. Since there is no termination for the first generation of DDR, large ripples are anticipated at the LPDDR receiver side, both inside and outside the SiP package. In addition, the LPDDR operates at the smaller 1.8 volts, as opposed to the traditional 2.5 volts. This further reduces the voltage swing and makes the receiver eye diagram appear even worse. Because of these factors, Sarcina Technology ran rigorous bidirectional channel simulation for the design of an SiP package with its PCB.

The engineering team imported a 3-D model of the LPDDR package from Cadence® Allegro® Package Designer software using the ANSYS ALinks for EDA translator and editor. The model was then ported to ANSYS HFSS to provide a full-wave S-parameter model for simultaneous noise switching analysis. The team then simulated this S-parameter model with read-and-write mode for data, strobe, address, command, control and clock signals for both internal and external LPDDRs.

Electrical simulation software gives designers the tools necessary to successfully design complex products the first time.



Simulated eye diagrams for internal and external LPDDRs under FF and SS corners. The FF corner has more ripples than the SS corner due to faster edge rate.



DDR3 differential clock net's topology for designed PCB and its daughter card from ASIC chip's controller to termination at daughter card. During the daughter-card layout, Ctt1 was inadvertently placed on the board, which shifted the clock and clock# crossover point in the eye diagram and violated hold time.

Eye diagrams at both the internal LPDDR die and external LPDDR chip were captured. The Sarcina team observed that, contrary to conventional thinking, the silicon wafer FF (fast P-type and fast N-type transistors) process corner had the worst eye diagram. This is because the fast edge rate at FF wafer corner introduces higher ripples. As a result, the eye diagrams are dramatically worse than the SS (slow P-type and slow N-type transistors) corner. In actuality, the SS corner has the best eye diagrams, even better than those of the TT (typical P- and N-type transistors) corner. This is due to the slower rising and falling edge rates, which help reduce ripples when no termination is present for LPDDR architecture. Through this simulation, Sarcina Technology's engineering team learned that it must use higher-grade LPDDR die, which requires smaller setup and hold time and, as an added benefit, gives more margin to the simulated eye diagram. Subsequent automatic test equipment debugging results showed that the higher-grade LPDDR was necessary for the SiP to pass DDR read-and-write tests. This simulation gave Sarcina Technology the rationale to order the higher-grade LPDDR wafer, which it would not have done without rigorous DDR channel simulation. The simulation helped the engineering team come up with a successful system on the first try.

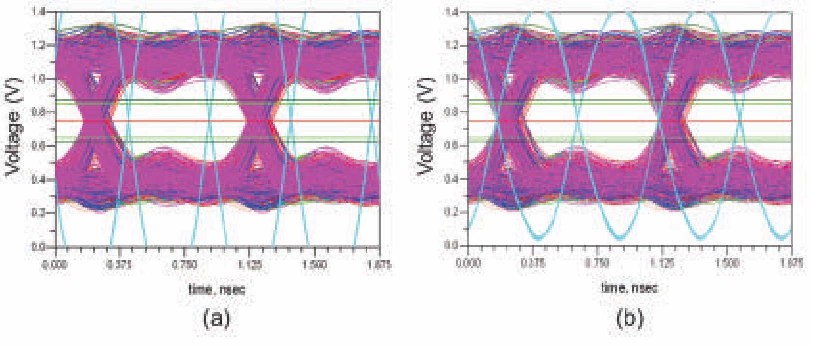
DEBUGGING A PCB DESIGN

Sarcina Technology's engineers also use electrical simulation in debugging PCB designs before the boards are assembled. This helps to avoid post-assembly lab debugging, which can be quite expensive and time-consuming. Data center customers demand first-time success in chip, package and PCB designs to meet the increasing demands of big data for large data transfers.

For example, consider the design of a DDR3 differential clock network topology for a potential PCB that includes a daughter card containing several DDR3 memory chips. The ASIC DDR3 controller (inside the ASIC chip) is on the main PCB board. During the daughter-card layout, a decoupling capacitor was inadvertently placed on the board. During post-layout DDR3 channel simulation for the address bus, the engineering team realized that the clock and clock# crossover point could not be positioned at the center of the address eye diagram because this created a hold-time violation.

After reviewing all simulation schematics and layouts in the PCB and its daughter card, the misplaced capacitor was revealed. Engineers used ANSYS SIwave to extract DDR3 electrical models for both PCB and daughter card. The extracted models allowed the team to perform what-if analyses with and without the capacitor to quickly identify the cause of the problem. Following removal of this capacitor from the simulation, the clock and clock# crossover point was repositioned close to the center of the eye diagram, which met both setup and hold-time specs.

Whether designing an LPDDR layout with ANSYS HFSS for simultaneous switching noise analysis or extracting DDR3 electrical models with ANSYS SIwave, Sarcina Technologies utilizes ANSYS simulation solutions to meet the ever-increasing demands of customers that develop the chips, packages and PCBs required by big data and the Internet of Things. Simulation is important to ensure first-pass success.



▲ DDR3 address simulated eye diagram with (b) and without (a) removal of capacitor Ctt1

ABOVE THE CLOUD

Cloud computing reduces by 80 percent the time required for a coupled CFD and structural simulation.

By Marius Swoboda, Head of Design Systems Engineering, and **Hubert Dengg,** Thermal Analyst
Rolls-Royce Germany, Dahlewitz, Germany

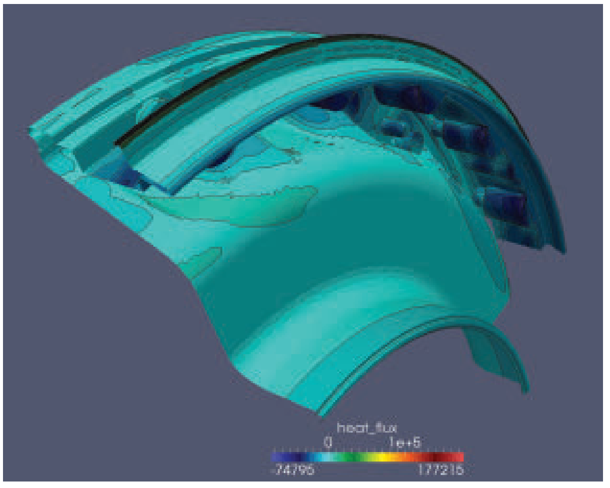
Rolls-Royce reduced the wall-clock time to perform the simulation by 80 percent.

Rolls-Royce uses an in-house, specialized structural code to determine the operating temperature of jet engine components such as turbine disks. The thermal boundary conditions for such an analysis are usually determined by mounting thermal sensors on the components and capturing heat flux measurements while the engine is running. One problem with this approach is that the thermal design of a new engine cannot begin until late in the product development process, when the first prototype becomes available. At this point, changes to the design are expensive, limiting what can be done to optimize thermal performance.

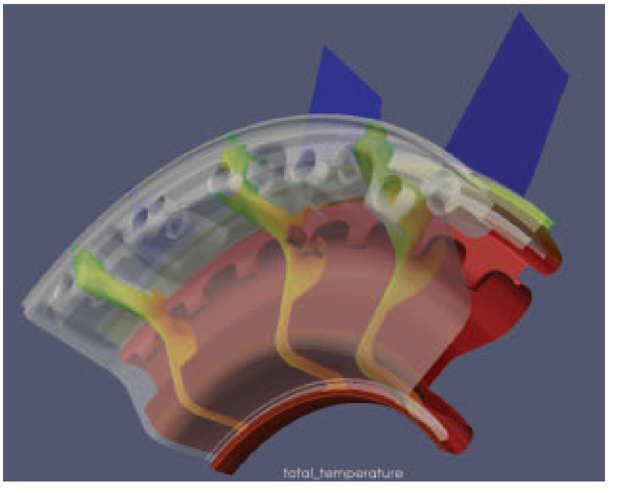
Rolls-Royce is a leader in the implementation of a new high-performance computing (HPC) cloud approach in which its structural solver is coupled with the ANSYS Fluent computational fluid dynamics (CFD) solver to provide heat flux predictions at many points on component walls without reference to a physical prototype. Performing this coupled simulation requires a high level of computational power because the solution is time-dependent. This means that CFD and structural solutions must be computed to convergence at each time step as the solution progresses. Rolls-Royce reduced the wall-clock time to perform the simulation by 80 percent by running the simulation on a hosted, shared HPC cloud system.

CHALLENGE OF HIGHER INLET TEMPERATURES

Engine manufacturers continue to increase turbine entry temperatures as they strive to improve engine efficiency. In this process, engineers must often redesign the engine's cooling and sealing systems to prevent the overheating of critical internal components. Rolls-Royce engineers determine the operating temperatures of these components by performing a thermal analysis with an in-house, specialized structural code. One of the inputs to the thermal analysis is the transient heat flux at an array of points on the walls of the components under study. Engineers believed that they could achieve major improvements in the design process by determining the heat flux with CFD, then coupling the CFD code to the structural



▲ Contours of heat flux, which are used as boundary conditions for structural code



▲ Contours of total temperature for the interstage cavity as outputs of the CFD calculation

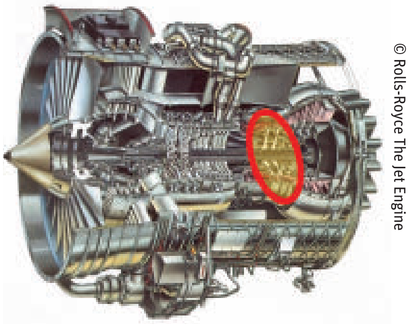
code to exchange the data at each computational cycle. The goal was to achieve an iterative loop with smooth exchange of information between the structural and CFD simulations so that the team could ensure consistent temperature and heat flux on the coupled metal–fluid domain interfaces. This continuous update of the heat transfer information to the components gives an accurate representation of the range of temperatures they will experience during startup and steady operation.

The conjugate heat transfer simulation process is very computationally demanding, especially when 3-D CFD models with more than 10 million cells are required. With internal HPC resources at full capacity, Rolls-Royce engineers considered using cloud resources to access HPC capabilities for this application. Engineers had to overcome several challenges. An interface between structural and CFD codes was available but had to be upgraded to allow for HPC. The other challenge was configuring the ANSYS Fluent process to run on several machines when called from the structural software. While a Fluent calculation spawned flawlessly on multiple cores, only one machine was used for the structural code within the coupling procedure. A change to the use of dedicated Fluent licenses in the cloud allowed the process to run independently of the in-house licensing and the queuing system. In the end, the licensing process ran much faster in the cloud than in-house.

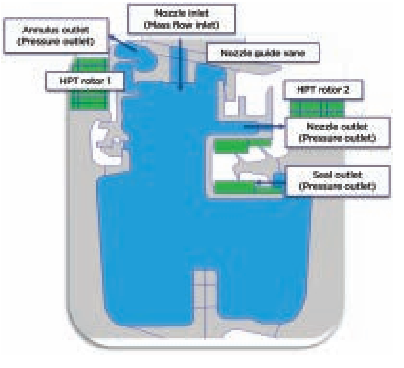
RUNNING SIMULATION IN THE CLOUD

Rolls-Royce selected CPU 24/7 GmbH & Co. KG to provide remote HPC computing power on demand. The computation was performed on an HPC cluster using Intel® Xeon® E5-2690 processors and FDR Infiniband® interconnects. The calculation was done in cycles in which either the structural solver or the Fluent CFD solver alternately ran and then passed data to the other when the cycle was completed. The CFD solution supplied heat flux at the walls, and temperature and swirl velocity as outputs to the structural code. The structural code provided temperature at the walls and inlets as boundary conditions for the CFD code. At each step, multiple iterations of CFD and structural solvers ran with solvers exchanging data until their calculated wall temperatures matched. The simulation ran for a total of 6,000 seconds of simulation time, which included startup, low-power and high-power engine operation. As expected, the bulk of the computational resources were consumed by the CFD calculation. The CFD part of the calculation was run on all 32 cores, while the structural part ran on only one.

CPU 24/7 contributed considerable expertise to the project, including how to set up a cluster, how to run applications in parallel based on a message passing interface (MPI), how to create a host file, how to handle the FlexNet® licenses, and how to prepare everything needed for turnkey



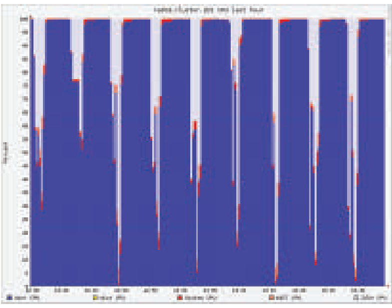
© Rolls-Royce The Jet Engine



▲ CFD model of high-pressure turbine interstage cavity

access to the cluster. During the whole process, CPU 24/7 supplied comprehensive and expedient technical support. It took only one month from the initial concept of executing the project on the cloud to the completion of the first calculation on the remote cluster. This rapid startup was possible because of the smooth collaboration between ANSYS and the CPU 24/7 team.

The results of the coupled CFD–structural simulation were validated with physical testing results. Because of the near-linear scalability of Fluent, running



▲ Cluster load during calculation cycles

the coupled fluid–structural simulation on the HPC cluster in the cloud was five times faster wall-clock time than running the problem on a local workstation. By outsourcing the computation workload to an HPC cloud provider, HPC resources were elastically provisioned and released. Rolls-Royce engineers were able to expand or shrink HPC capacity as needed, thus increasing their operational IT efficiency and better utilizing HPC resources. For example, the availability of cloud computing resources makes it possible to scale up HPC to run even bigger models that provide more detailed insights into the physical behavior of the system.

There is currently no physical way to determine the performance of a proposed cooling and sealing design until the hardware is built and tested. At that point, so much time and money have been invested in the design that changes are very expensive. It is also impossible to evaluate more than a few alternatives using the build-and-test method. Simulation is the only answer. One significant advantage of running a coupled structural–fluid simulation in the HPC cloud is the potential to iteratively optimize the entire cooling and sealing system design in the early stages of the product development process. An experiment can be designed to explore the complete design space, and then engineers can select the best possible design for prototyping and testing. Rolls-Royce is aggressively pursuing this HPC cloud approach, which has the potential to achieve significant improvements in jet engine performance.

OPTIMIZING BUSINESS VALUE IN HIGH-PERFORMANCE ENGINEERING COMPUTING
ansys.com/83cloud

Running the coupled fluid–structural simulation on the HPC cluster in the cloud was five times faster wall-clock time than running the problem on a local workstation.

EYE IN THE SKY

A small engineering team designed, verified, generated and integrated 125,000 lines of code to control an unmanned aerial system using ANSYS SCADE in one-third the time required had the code been written in C.

By Giuseppe Cinà, Flight Control Systems Manager, Piaggio Aero Industries, Genoa, Italy
Amar Bouali, V.P. South Europe, Turkey, MEA Operations, Esterel Technologies, a wholly-owned subsidiary of ANSYS

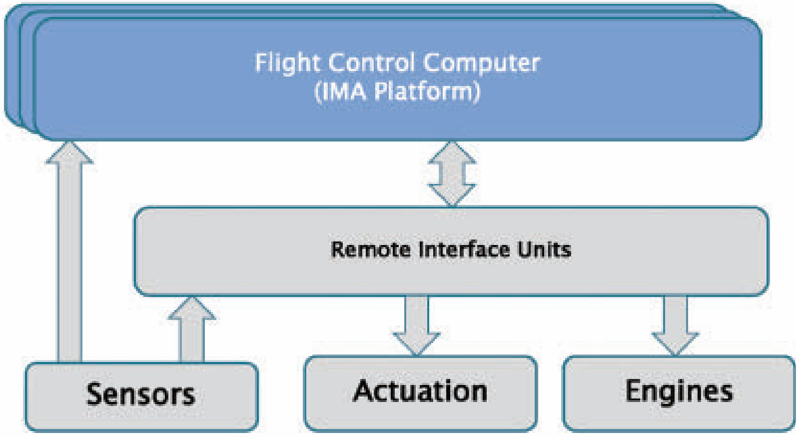
P.1HH HammerHead shown in first flight

The use of unmanned aerial systems (UASs) for intelligence, surveillance and reconnaissance (ISR) missions has shown explosive growth. As their value continues to be demonstrated, this growth shows no sign of slowing. The UAS sector must address a number of key technical and manpower challenges in developing autonomously controlled aircraft. Engineers from Piaggio Aero faced the challenge of transforming the company's conventional manned P.180 Avanti II executive jet into a UAS. The vehicle command-and-control architecture needs to be certified against first-generation requirements while supporting a design road map that foresees growing functionality to support different configurations. This job had to be done with a strictly controlled number of engineers to limit overhead and succeed in a very short time. Piaggio engineers accomplished these goals with a new development process in which ANSYS SCADE models were created from scratch, or, if Matlab/Simulink® models were available, they were translated via the SCADE Suite Gateway for Simulink®. From the SCADE model, the embedded source code was generated automatically with the SCADE KCG qualified code generator. The vehicle control and management system (VCMS) — the digital infrastructure performing aircraft command and control — was tested continually, first at the model phase, then on the host, and

The first flight of the aircraft was successfully completed less than two years after the project began.

finally in the target environment so that the team could identify problems and correct them at the earliest possible point.

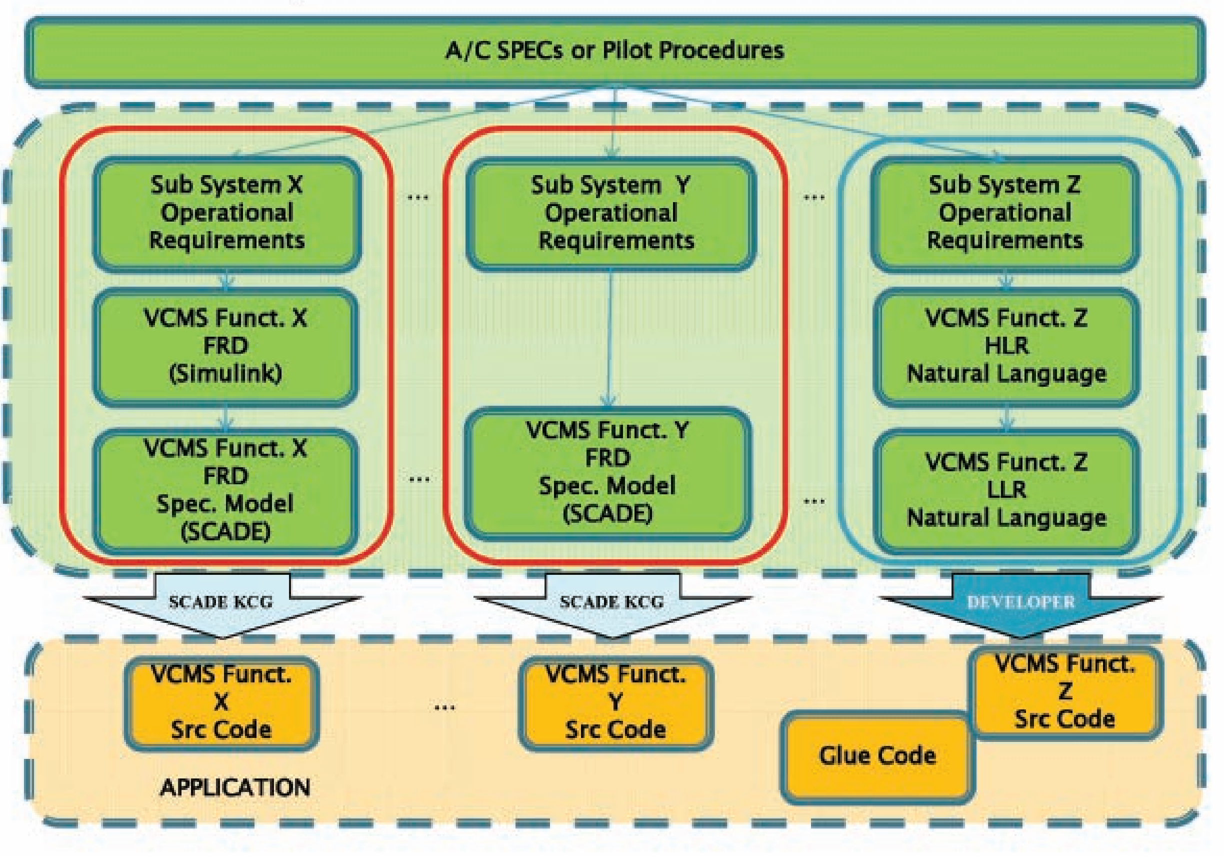
Piaggio Aero Industries S.p.A. is a multinational aerospace manufacturing company headquartered in Genoa, Italy. It designs, develops, constructs and maintains aircraft, aero-engines and aircraft structural components. Powered by two Pratt & Whitney Canada PT6-66B turboprop engines, Piaggio's newly developed P.1HH HammerHead will provide sophisticated standoff (deployed at a distance) capabilities for any surveillance and security need. The VCMS manages flight control, propulsion, electrical power generation and distribution, landing gear, braking, ice detection and protection, navigation and communications systems. Partitioning techniques were used to create a segregated environment in which software applications of each function run without interfering with each other to avoid propagating failures.



▲ VCMS architecture

DEVELOPING SOFTWARE REQUIREMENTS

In the first months of the project, the team developed the engine and flight control laws; it also created the other requirements for the embedded software. High-level requirements for the VCMS were available in several different formats. Systems engineers collected some requirements in textual form as functions, interfaces and redundancies. Other requirements were captured in text from operating manuals such as the P.180 Pilot Operational Handbook. Control laws, algorithms and equations involved in flying the plane were written, simulated and validated in MathWorks® Simulink. Requirements were generated in the IBM®



▲ P.1HH development process

Rational® DOORS® requirements management environment. Test cases were also written in DOORS and linked to operational requirements using the SCADE Requirement Management Gateway. For each test case, test steps and expected results were defined.

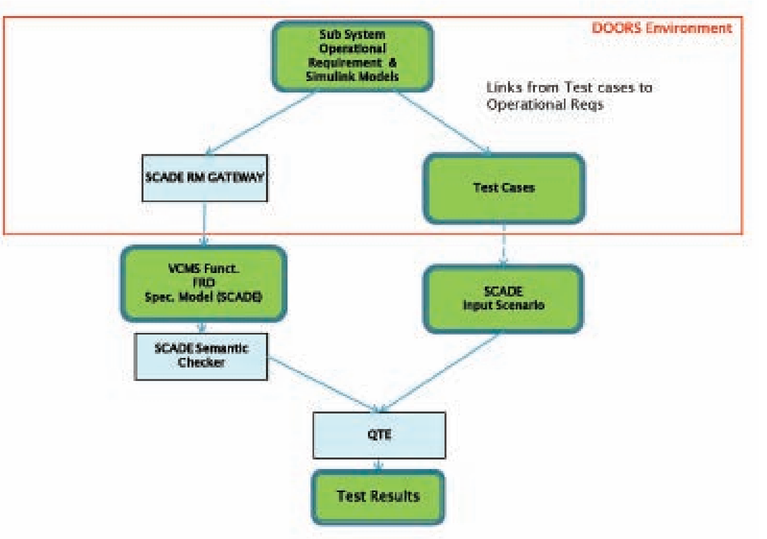
For this project, the software must comply with DO-178B, the de facto standard used to qualify all avionics software by the FAA, EASA and other certification authorities. Piaggio selected ANSYS SCADE as the development environment for the VCMS, since SCADE automatically generates source code from the model and minimizes the effort required to verify that the source code corresponds to the system model. The ANSYS SCADE KCG code generator is qualified as a DO-178B development tool, so conformance of the code to the input model is trusted, eliminating the need for verification activities related to the coding phase. SCADE's model-based methodology enables system engineers to model each function autonomously and check its performance on a host computer before the real hardware is available.

CREATING MODELS

SCADE models were created based on functional requirements from scratch by systems engineers for the textual documents, and automatically via the Simulink Gateway for the existing Simulink models. The SCADE Requirements Management Gateway was used to link the requirements to the embedded system design in the SCADE model. Engineers employed the SCADE Semantic Checker to verify the semantics of the model. Problems were identified and resolved in the host on the PC environment rather than in the much more expensive and complicated target hardware environment. A small portion of the code, primarily low-level layers such as input/output, was developed in C using traditional methods.

To ensure that the Simulink model was correctly translated to the SCADE environment, Simulink test vectors were translated into the SCADE environment. The test cases were translated to SCADE Input Scenarios. Then the test vectors were run in both Simulink and SCADE, and the results were compared to ensure that the translated SCADE model had the same functional behavior as the original Simulink model.

SCADE USAGE FOR UNMANNED AIRCRAFT VEHICLES
esterel-technologies.com/83piaggio



▲ SCADE model validation process

SOFTWARE VERIFICATION

DO-178B verification requires proof that the functional tests performed by the test vectors fully cover model functionality. The SCADE Model Test Coverage (MTC) tool checked the model coverage and identified several areas that were lacking. Additional tests were designed and performed to provide the needed coverage.

Verification activities exponentially increase as the number of inputs of each model grows and as the number of models increases. In the early stages of the project, test vector generation, validation and configuration were issues. SCADE LifeCycle Qualified Test Environment (QTE) provided a solution by automatically running the tests in the host environment, comparing the results to the expected values and highlighting any errors.

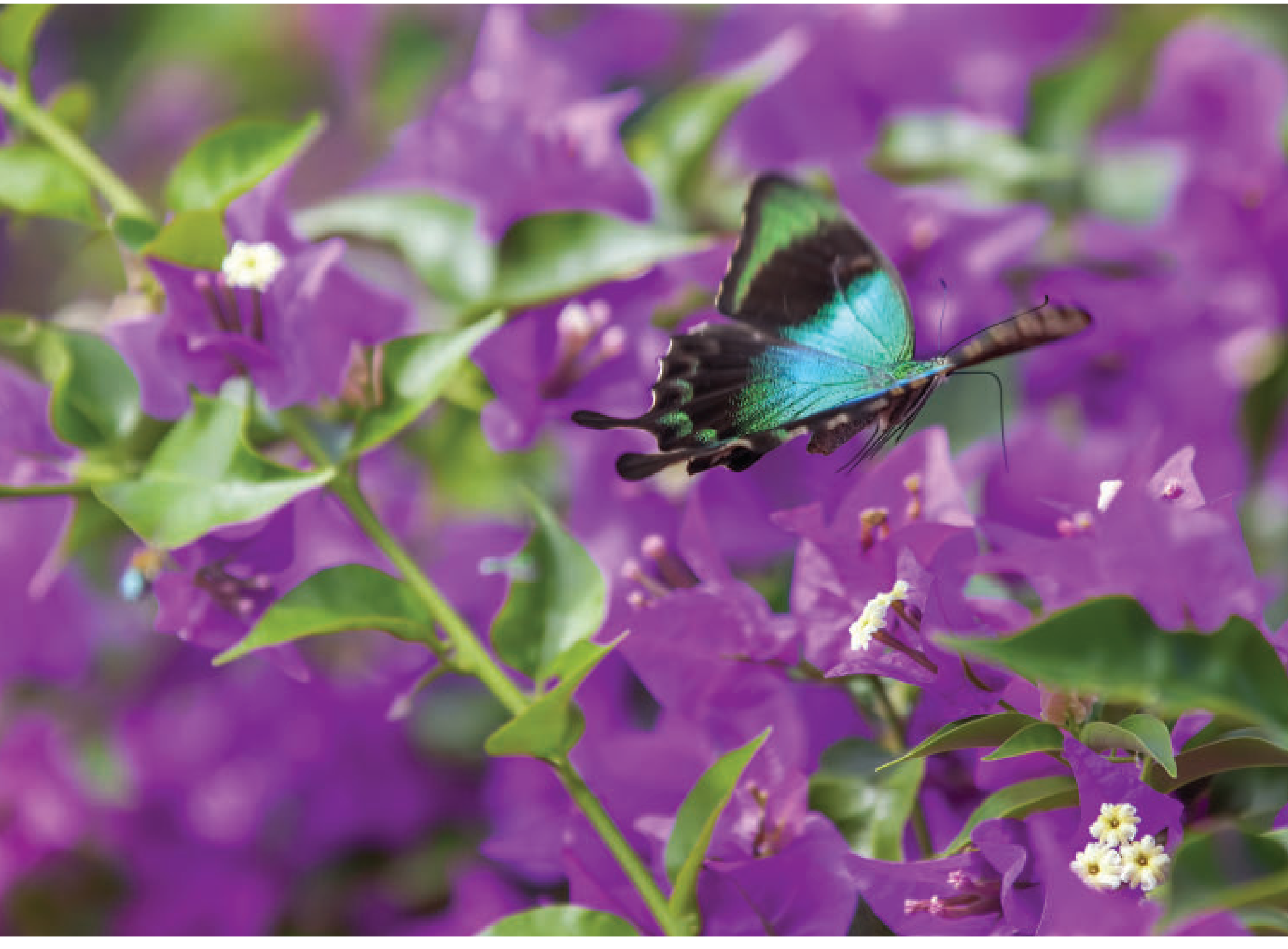
Similar activities were performed on the target computer, sending test vectors into the executable code generated from the models. Piaggio engineers wrote a simple test application tool that runs on the target and plays a role similar to QTE by running the application with the SCADE input scenario then comparing results with the output generated by the same application and input on the host.

SYSTEM INTEGRATION

Models to handle different functional aspects of the VCMS were progressively integrated on the host computer to build a virtual VCMS to check interoperability of the applications well in advance of system integration. These verification activities were used to identify and solve many integration problems even before performing system integration on real hardware. As a result, the problems found during system integration were small in number, and all were mainly due to hardware/software/subsystem integration issues rather than to design errors. Once system integration was completed and the final tests executed, data from the real world were fed into the test vectors to further verify the model.

The entire project was completed in about 18 months, starting with model development performed directly by the system engineers and proceeding to compilation, integration and verification of the approximately 125,000 lines of source code that comprise the VCMS. The working team — in terms of equivalent full-time manpower — was limited to less than 20 engineers (system and software) who worked in tight coordination from the early design stages up to final system integration to meet the challenging target. As a result, the VMCS was developed and verified in an estimated one-third the time that would have been required had the code been handwritten.

The first flight of the aircraft was successfully completed in November 2013, less than two years after the project began. The VCMS worked perfectly. The P.1HH configuration will grow through incremental software releases that will add new functionalities to expand mission capabilities of the P.1HH. Λ



ON THE WING

Butterfly wings generate far more lift than can be accounted for by steady-state, non-transitory aerodynamics.

By Sutthiphong Srigrarom, Associate Professor, Aerospace Systems, University of Glasgow Singapore, Singapore

The delicate butterfly is well known for its ability to fly great distances. The wing structures of monarch and swallowtail butterflies are a marvel of aerospace design, allowing for a wide range of mechanisms to generate force: wake capture, two different types of leading-edge vortex, and active and inactive upstrokes. Aerospace engineers at the University of Glasgow became fascinated with this and saw a perfect opportunity to capture workings of this natural design in their ongoing development of a butterfly-like ornithopter (flapping wing) micro-aerial vehicle (MAV).

Engineers selected the butterfly species based on the requirements for an MAV: agility and in-flight stability. Monarch butterflies

DESIGNING A FLAPPING-WING-TYPE MICRO AERIAL VEHICLE USING ANSYS
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The wing structures of monarch and swallowtail butterflies are a marvel of aerospace design.

have the ability to turn on a dime while evading predators, while the swallowtail's hind wings sport unique streamers that appear to act as stabilizers. Both wing types generate far more lift than can be accounted for by steady-state, non-transitory aerodynamics, so Glasgow engineers decided to focus on transient analysis to discover precisely what flow interactions enable butterfly wings to perform so effectively.

The work used ANSYS Fluent to study the fluid flow. Engineers conducted a fully 3-D unsteady direct numerical simulation (DNS) of Navier–Stokes equations to completely capture all the structures of the flow generated by the wing motion. The computer chosen to run the simulations was a 64-bit Intel® Core i7-2600 CPU at 3.4 GHz with eight processors and 16 GB of RAM.

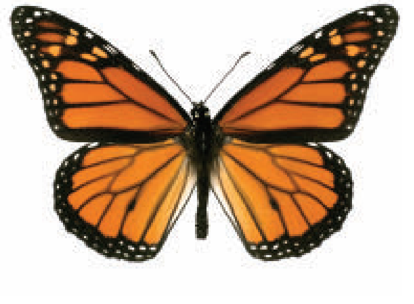
The team treated the butterfly models as rigid structures. For fluid-flow studies, engineers made the simplifying assumption that the butterflies' bodies and wings exhibited no deformation during flight. A half-model of each butterfly was used to reduce problem size, and the fluid domain around each model was extended to 20 to 40 times the butterflies' bodies in all directions. The mesh was unstructured, with approximately 10 million elements clustered around the wings. Engineers used observations of real natural flight to model the flapping-wing motion during translation (forward motion) and hovering. The effective Reynolds number ranges of the flow for both flight modes based on body length, maximum wingtip speeds and free stream velocity were about 500.

During CFD analyses, the flight behavior of the monarch butterfly served as the standard for comparison with that of the swallowtail butterfly because the differences in the flow patterns allowed researchers to isolate stabilization effects of the tail streamers. Both butterflies have a high flight velocity, with a high-amplitude, low-frequency wing stroke. Engineers observed from real flight that the wing strokes were roughly perpendicular to the body axis. This allowed the butterfly fluid model to be solved in a frame that rotated about the body axis. The midpoint of the power stroke (down stroke) at $\varphi = 0$ degrees was taken as the start-point for the simulations, which captured a wing beat range from –80 degrees to +80 degrees at a frequency of 1 Hz.

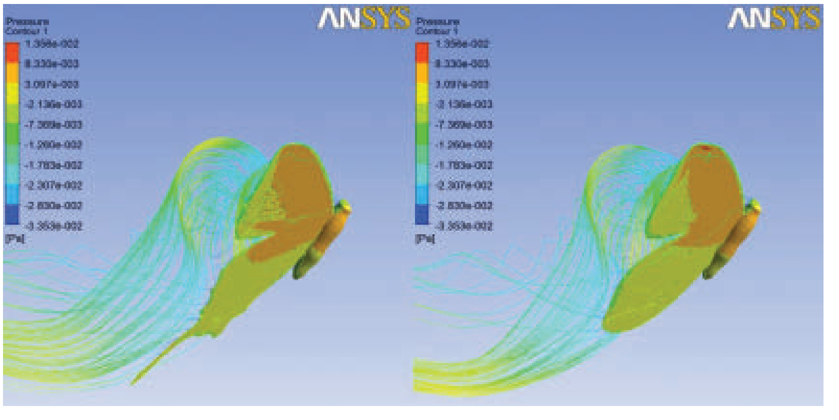
The CFD analyses showed that wing beats during the hovering motion created

Both wing types generate far more lift than can be accounted for by steady-state, non-transitory aerodynamics.

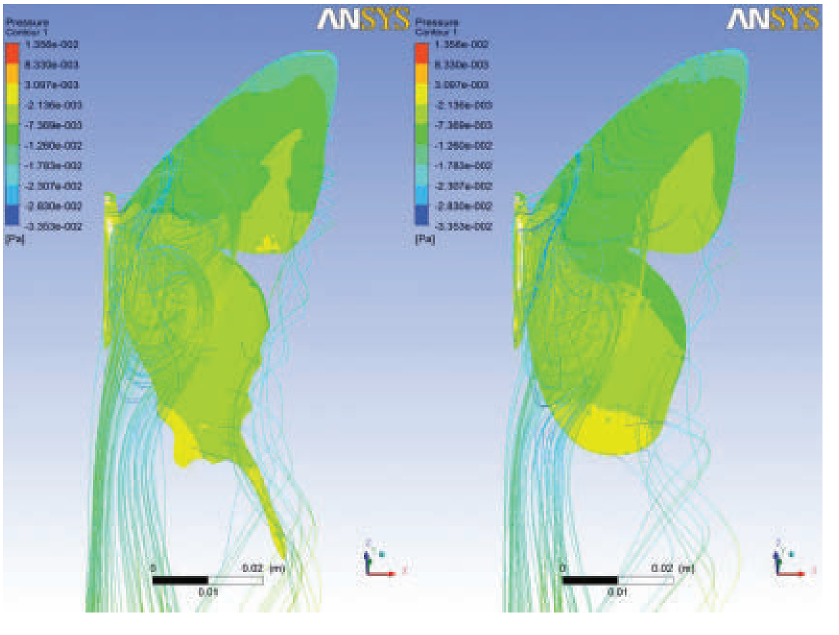
Swallowtail butterfly



Monarch butterfly



Comparison of streamlines of both butterflies side-by-side: isometric view, front



Comparison of streamlines of both butterflies side-by-side: 3-D view, top an intensive, stable leading-edge vortex along the leading edges of both fore- and hind-wings. This vertical vortex rotates counterclockwise toward the inside back of the wing. Simultaneously, airflow that passes directly through the gap between the wings at the beginning of the power stroke moves along the axis of the vertical vortex ring and begins to drive it backward. There is a horizontal stopping vortex downstream of the butterfly caused by deceleration of the wings at the bottom of the previous stroke. During flight, both vortices merge into a new attached horizontal vortex ring generated by the continued flapping of the wing. The overall mechanism is similar to wake-capturing and is responsible for the unprecedented lift generated by the downstroke of the butterfly's wings.

Results from forward flight motion were discovered to be quite similar, with the main difference being that the leading-edge vortex ring was tilted. Researchers observed that the subsequent vortex formation pattern differed as well. For forward flight, the vertical vortex ring moves quickly backward because of convection caused by forward motion. At the bottom of the stroke, the wings shed a horizontal vortex ring downward and backward. Unlike in hovering flight, in which the horizontal ring merges with the vertical one and is attached near the edges of the hind wings, in migration flight, deceleration of the wings at the bottom of the stroke is accompanied by vortex ring shedding. Leaving the wings, the horizontal vortex ring moves downward and backward.

The aerodynamics of the swallowtail butterfly were similar to that of the monarch in both flight conditions. Dominant leading-edge vortices again emanated along the wings' leading edges. Airflow passes through the gap between the flapping wings to move along the axis of the vertical vortex ring. The most interesting finding of the study was the large impact of the streamers on the flow structures produced during flight. Streamers at the lower and outer corner of the swallowtail's hindwings introduce additional horseshoe-like vortices around the edge of the streamer. Wake vortices become aligned behind the wings by these additional horseshoe vortices, making the swallowtail butterfly flight more stable.

Engineers also found that the leading-edge vortices that are generated by the swallowtail's wings are enlarged by the

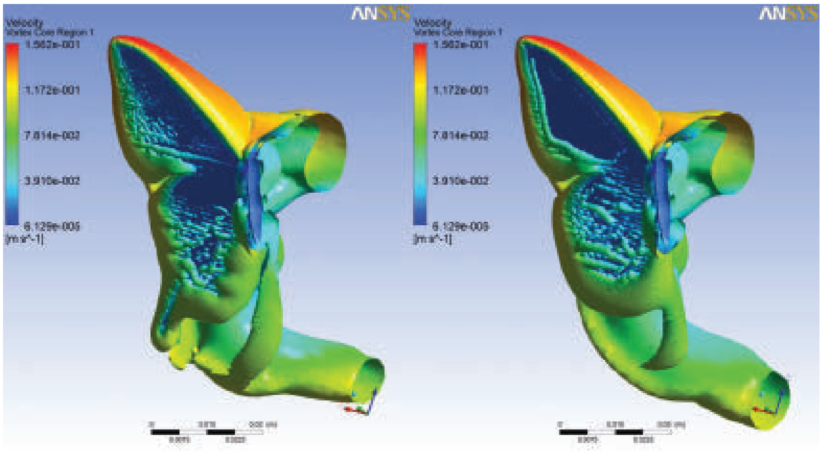
The unconventional aerodynamics of butterfly wings will greatly assist in ongoing refinement of Glasgow's MAV.

Force and moment generated by both butterflies during hovering motion (all values ± 5 percent)

Hovering motion, flaps at 1 Hz	C_L	C_D	C_M
Monarch butterfly	0.041	0.032	0.040
Swallowtail butterfly	0.074	0.075	0.072

Force and moment generated by both butterflies during forward motion (all values ± 5 percent)

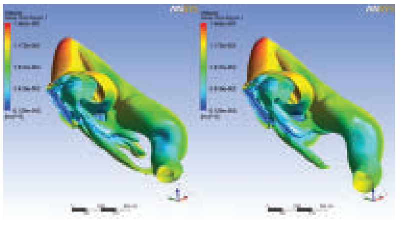
Forward motion, flaps at 1 Hz	C_L	C_D	C_M
Monarch butterfly	4.571	4.980	4.868
Swallowtail butterfly	5.233	6.172	5.113



Comparison of vortex structures of both butterflies side-by-side: isometric view, below

stabilization, creating a more effective wing. The forces and moments of swallowtail wings are approximately 20 percent greater than those generated by monarch wings, even though the area difference between the two wings is only 5 percent. Since there were few other differences between the two models, researchers concluded that the significant increase in forces and moments must result solely from the streamers.

Both CFD studies gave engineers increased insight into the flow patterns required for a light, powerful wing design beneficial to the continued development of MAV technology. The unconventional aerodynamics employed by butterfly wings revealed by this study will greatly assist in the ongoing refinement of Glasgow's MAV.



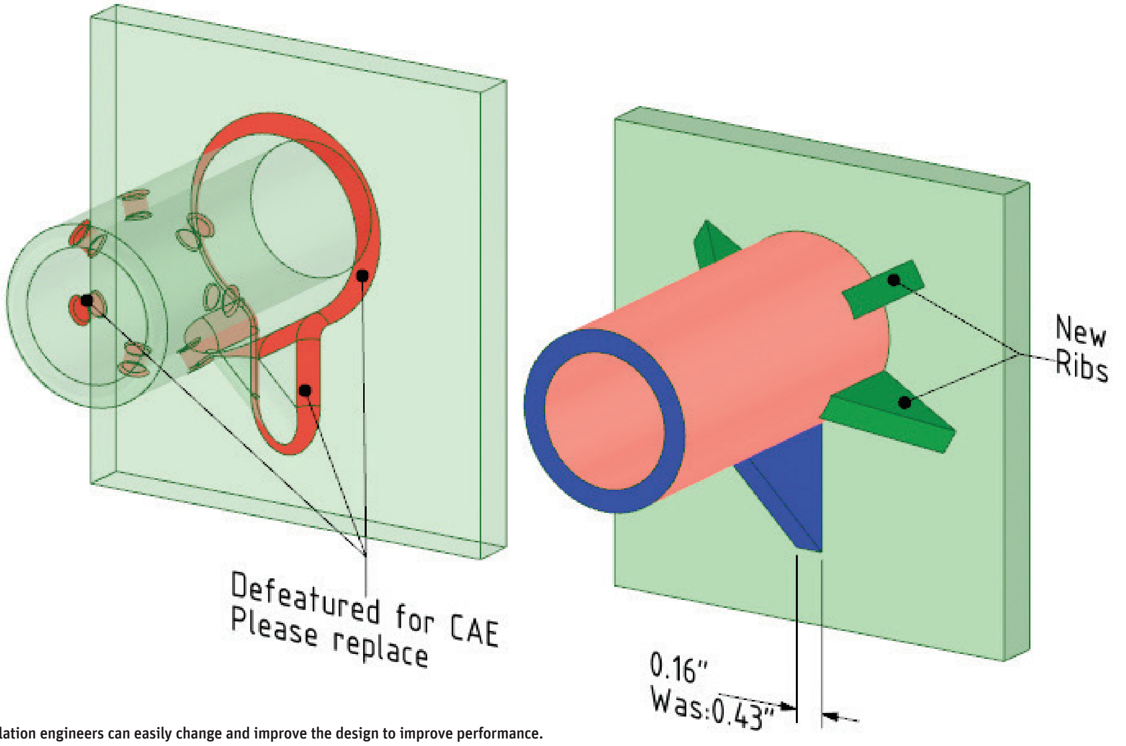
Comparison of vortex structures of both butterflies side-by-side: isometric view, front

Support for this project has been provided by ANSYS channel partner CAD-IT Consultants (Asia) Pte Ltd.

BLENDING DESIGN AND SIMULATION

SpaceClaim and ANSYS bring innovative design and analysis closer together.

By Rebecca Swensen, Senior Product Marketing Manager, ANSYS

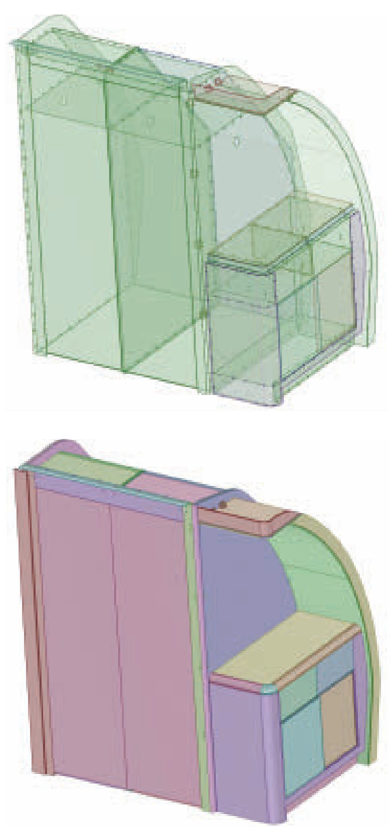


Simulation engineers can easily change and improve the design to improve performance.

SpaceClaim 3-D direct modeling software — available from ANSYS for several years and now part of the ANSYS product family — is a powerful tool for creating, importing and working with 3-D geometry. It has a simple and robust user interface that includes tools to defeature both parts and assemblies prior to meshing and solving. SpaceClaim has the power to simplify and automate what has traditionally been the time-consuming process of preparing geometry for use in a simulation system. With SpaceClaim, engineers can author new concepts and more easily use simulation to iterate on designs and drive innovation.

Increased speed and pressure from competition is compelling organizations to find easier, more effective ways to

SpaceClaim 3-D direct modeling software was recently added to the ANSYS product family.



▲ SpaceClaim makes it easy to create solids for analysis with automated fixes and simple tools for defeaturing.

develop innovative designs. By changing some workflow practices, an engineer can obtain workable geometry early in the design cycle. By performing simulation earlier in the design process, performance data can be built into the design process before key features have been determined to save product development time and costs.

SpaceClaim's defeaturing capabilities quickly create ideal models for meshing in a fraction of the time required by a traditional computer-aided design (CAD) tool. The software was created to enable those without CAD expertise to work with 3-D models, make the needed changes and resume their primary job function. SpaceClaim enables companies to perform analysis up front in the design process.

CONCEPT MODELING TOOLS DRIVE UPFRONT DESIGN EXPLORATION
ansys.com/83blending

HOW SPACECLAIM WORKS

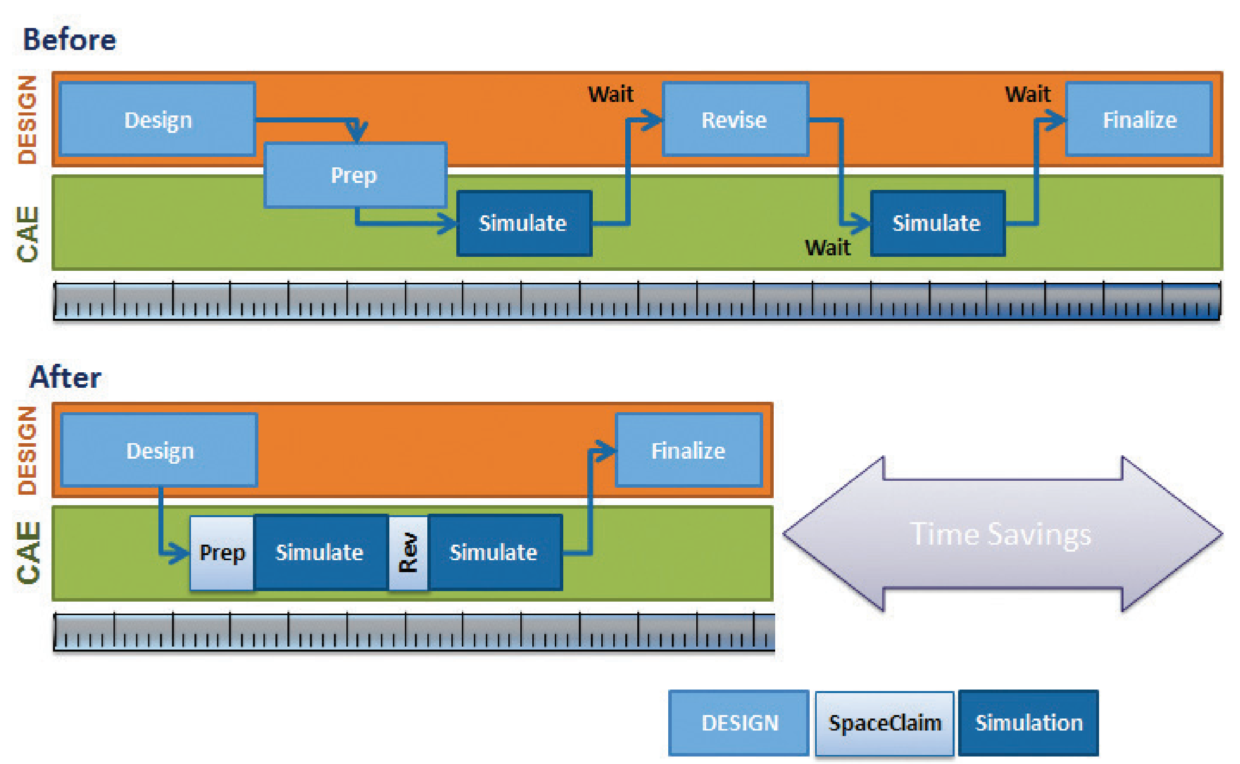
To help with bad geometry, SpaceClaim makes model repair easy by using a fast detect-and-repair approach to fix files. The direct modeling software can automatically fix common issues when opening files and also provides interactive tools for deeper repairs. If parts are missing some geometry, SpaceClaim's direct modeling technology will blend seamlessly with repair tools to reconstruct data. A CAD specialist isn't needed to execute changes; analysts can make the changes themselves and communicate the edits as needed.

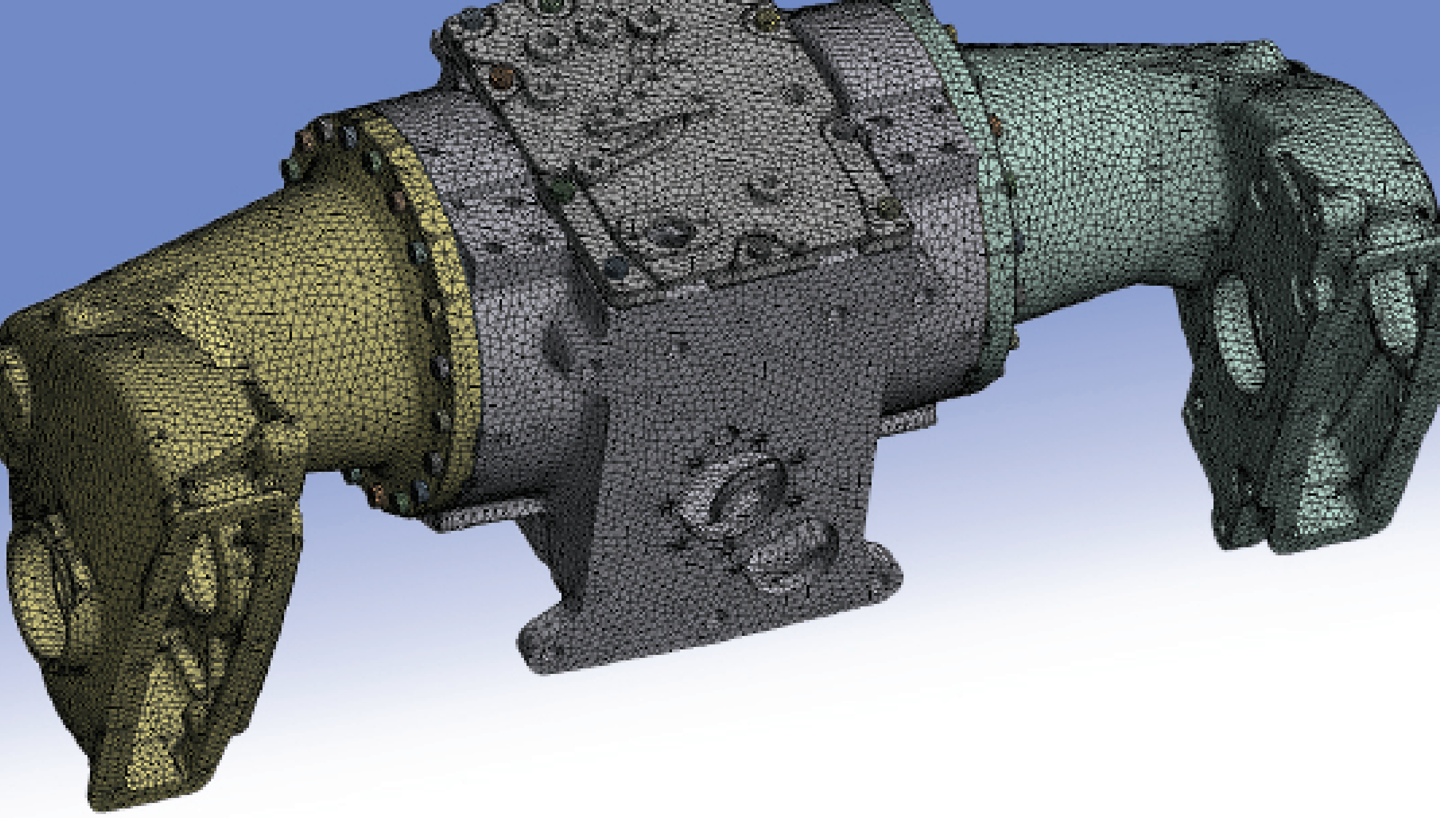
The core of SpaceClaim is four simple tools that accomplish most of the geometry editing:

- Pull: Add or remove from the design
- Move: Modify the design
- Combine: Cut solids
- Fill: Remove and clean geometry

For many common repairs, the automated detect-and-repair functions do most of the work and reduce the need for manual patching.

Speeding model preparation for simulation is an important part of implementing and realizing the full benefit of simulation-driven product development.





GPUs SPEED THE SOLUTION OF COMPLEX ELECTROMAGNETIC SIMULATION

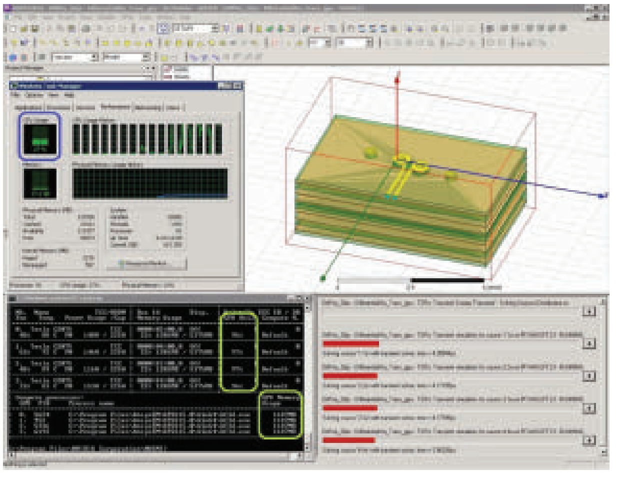
The ANSYS HFSS transient solver leverages NVIDIA's leadership in GPU computing to enable quick solutions for transient electromagnetic simulation.

By Hsueh-Yung (Robert) Chao, Lead R&D Engineer, and
Stylianos Dosopoulos, Senior R&D Engineer, ANSYS

Transient electromagnetic (EM) analysis is indispensable for modern electronic design. Since the ANSYS HFSS transient solver's debut, it has been applied to a variety of design challenges in the electronics, semiconductor, energy, automotive, aerospace and defense industries. The product provides robust solutions for applications related to electromagnetic interference and compatibility (EMI/EMC), signal integrity, time-domain radar cross section (RCS), time-domain reflection/transmission (TDR/TDT), lightning strike and ground penetration radar (GPR). The HFSS transient solver is most beneficial for applications that require time-domain intuition and field visualization. It can also perform frequency-domain analyses such as S-parameters and frequency-domain far fields.

There is a growing interest in studying the electrostatic discharge (ESD) on touch screens of mobile handheld devices. ESD is often considered the top reason for post-shipment failure of solid-state electronics. This phenomenon is inherently transient and well suited for analysis by a transient EM solver for field visualization. By simulating field strengths on sensor pads, engineers can determine if thin-film oxide will potentially be damaged by dielectric breakdown at hot spots. Because of the miniature scale of the structures and extremely short duration of discharge, it is difficult to obtain reliable prediction through measurement.

In addition to analyzing structures at millimeter scales, the HFSS transient solver can solve such large-scale problems as the spilled fields induced by switching extra/ultra-high voltage (EHV/UHV) bus charge currents in a power substation. The transient spilled fields pose a potential safety hazard to personnel and equipment and cannot be predicted by steady-state



▲ Network analysis of differential stacked vias on four GPUs. Simulation jobs are run in parallel as shown by the progress bars and NVIDIA System Management Interface (nvidia-smi). The model was discretized into 68,401 tetrahedrons.

Transient EM analysis is indispensable for modern electronic design.

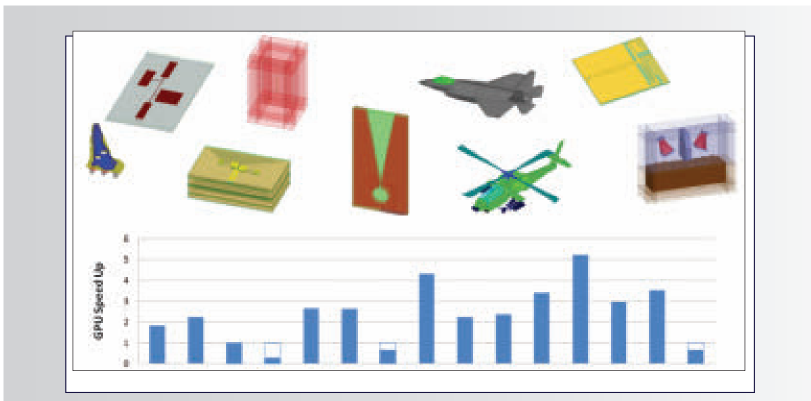
Expanded GPU Support Across Multiple Physics

To leverage cutting-edge hardware and deliver faster engineering simulation technology to users, ANSYS has teamed up with NVIDIA® to develop and release a GPU-accelerated computational fluid dynamics (CFD) solver. The result of a multi-year strategic partnership, this new solver addresses customer demand for increased speed and the ability to handle larger, more complex CFD simulation models. Available in ANSYS 15.0, the solver — and a new HPC licensing that enables all HPC users to take full advantage of GPU technology — broadens support for GPU acceleration within the ANSYS portfolio. GPUs can now speed up fluids, structural and electromagnetic simulations to increase the value of ANSYS HPC capabilities.

— Wim Slagter, Lead Product Manager, ANSYS

ACCELERATING ANSYS FLUENT 15.0 USING NVIDIA GPUs
ansys.com/83GPU

electromagnetic analysis. It is therefore highly advantageous to simulate different options of bus layout and equipment placement during the early stage of plant planning. By extracting the resistance, inductance, capacitance and conductance (RLCG) equivalent circuits of buses and switches through ANSYS Q3D Extractor and performing broadband SPICE circuit simulation using ANSYS Designer, engineers can obtain time-varying voltage sources for an HFSS transient simulation.



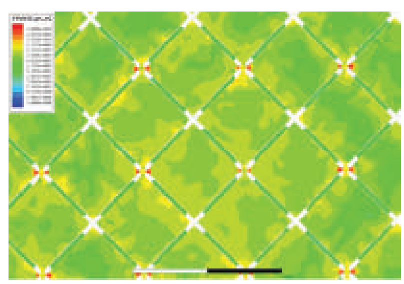
▲ ANSYS HFSS transient benchmarks on one NVIDIA Tesla K20 compared with eight cores of Intel Xeon X5675. Only nine of the 15 benchmark structures are shown in the figure. Dotted lines indicate cases in which the GPU did not provide speedup and CPUs were automatically used.

[redacted]

GPU ACCELERATION

The ANSYS HFSS transient solver's engine is based on the discontinuous Galerkin time-domain (DGTD) method, which is especially compatible with parallel execution on general-purpose graphics processing units (GPUs) with thousands of cores. With advances in GPU acceleration, more than four teraflops of computing power can be achieved on a single GPU that consumes less than 240 watts of electric power. Release 15 of the ANSYS electromagnetics suite enables engineers to leverage NVIDIA® CUDA™ technology for GPU computing to accelerate the HFSS transient solver. The GPU-accelerated solver can typically achieve two-times speedup on one NVIDIA Tesla K20 versus eight cores of Intel® Xeon® X5675. As a general rule, problems that require intense computational effort tend to result in higher speedup factors. In benchmarks of 15 examples, a maximum speedup of 5.2 times was achieved. Moreover, the solver can detect cases in which GPUs may not provide speedup and automatically fall back to CPUs. In those cases, there is no significant performance decrease since CPUs using OpenMP multithreading are employed.

The speedup with GPU acceleration scales linearly with respect to the number of GPUs when the simulations are run with multiple HPC tasks for parametric sweeps or network analyses with multiple excitations. For example, if the transient analysis of a four-port network takes 40 minutes in serial on one GPU, the simulation time is reduced to around 10 minutes with four GPUs running in parallel. When solving four excitations consecutively, the speedup of one NVIDIA Tesla C2075 versus eight cores of Intel Xeon E5-2650 is 7.2 times. Therefore, the overall speedup is 28.9 times when all four NVIDIA Tesla C2075s are used. The assignment of multiple GPU jobs is fully automatic and requires no user intervention. The HFSS transient solver uses NVIDIA's exclusive process compute mode to assign one process to one GPU. Therefore, engineers will encounter no issues of load balancing or multiple HFSS processes competing for hardware resources on a single GPU.



▲ Strong electric fields (red) on the bridges between sensor pads of the touch screen of a handheld device cause dielectric breakdown of indium-tin-oxide (ITO) thin films.

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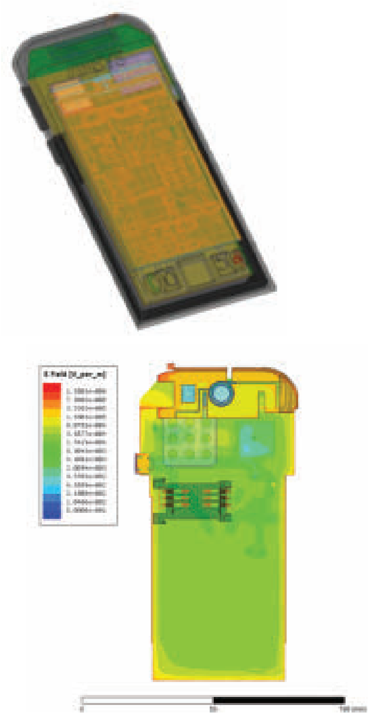
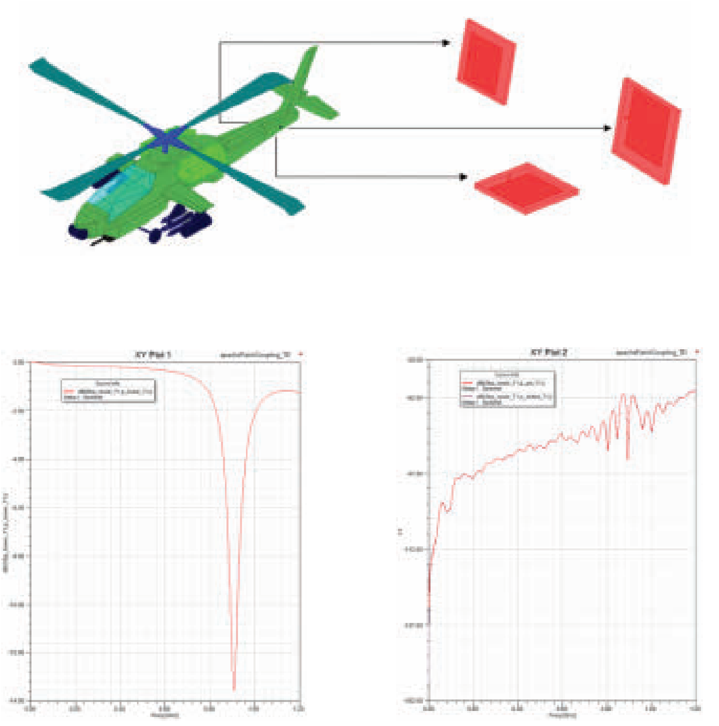
For example, simulation speedup occurs when performing power-surge analysis of a smartphone using the HFSS



A smartphone for transient field analysis on CPU, memory, GPS and Bluetooth ports due to power surge during battery charging. The model was discretized into 1,093,376 tetrahedrons.



Three patch antennas placed on the tail of a helicopter (top) and their S-parameters from DC to 1.2 GHz (S11 bottom left, S12 and S13 bottom right). The length, height and wingspan of the helicopter are 17.73 meters, 4.05 meters and 5.23 meters, respectively. The model was discretized into 549,247 tetrahedrons.

transient solver on a GPU. One NVIDIA Tesla K40, using 5.99 GB GPU RAM, speeds up the simulation 4.8 times when compared with eight cores of Intel Xeon E5-2687W. For signal integrity analysis of the printed circuit board, one NVIDIA Tesla C2075, using 3.98 GB GPU RAM, is twice as fast as eight cores of Intel E5-2650.

Moreover, when applying the transient solver to analyze the antenna coupling on a helicopter, the speedup of one NVIDIA Tesla K40 versus eight cores of Intel Xeon E5-2687W is 4.5 times, and the GPU RAM requirement is 4.35 GB. In all cases, the GPU solver requires less memory than its CPU counterpart. The frequency-domain S-parameters are calculated dynamically during the transient simulation. The simulation shows the resonant frequency of the patch antenna at 0.91 GHz and low mutual coupling (below –60 dB) between the antennas.

INSTALLATION AND SETUP

To access GPU acceleration, you must have NVIDIA GPUs and drivers installed on your computers and clusters. GPU acceleration in the ANSYS HFSS transient solver is officially supported with the Tesla and high-end Quadro series cards. For optimal performance, GPUs used for running simulation jobs should not be simultaneously used for visualization jobs. Only GPU cards with CUDA compute compatibility 2.0 and above should be used. To improve the speedup of transient field visualization, the GPU cards should be installed on a system with PCI-E 3.0 slots. A mixture of interface cards with lower PCI-E versions may result in the data not being transferred from GPU to CPU at the highest speed.

Before running HFSS transient simulations, it is important to ensure that GPUs are set with error correction code (ECC) disabled for performance, Tesla compute cluster (TCC) enabled for remote execution, and exclusive process enabled for GPU distributed computing. The GPU processor and memory usages are monitored through NVIDIA's utility program nvidia-smi.

Thanks to Rickard Petersson and Matt Commens for their valuable input to this article. Application examples courtesy Jack Wu, Ally Liu and Sara Louie.

The ANSYS electromagnetics suite allows you to leverage NVIDIA CUDA technology for GPU computing to accelerate the HFSS transient solver.

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